CHAPTER 4
A 3-phase 4-wire 4-leg voltage sags compensator

4.1 Introduction

Recently, the voltage sag compensators have been unable to handle neutral current caused by unbalanced and/or nonlinear loads or unbalance source. This thesis presents a 3-phase 4-wire 4-leg voltage sag compensator based on three dimensions space vector modulation in *abc* coordinates which can handle the neutral current under voltage sag and nonlinear load conditions. The topology of this hardware consists of voltage sag detector, DC/DC converter, solid state transfer switch, 4-leg inverter. The main advance of 4-leg inverter topology and algorithm lie in and extended range for the zero sequence voltages and currents. The space vector modulation algorithm use of *abc* coordinates is must simpler and more intuitive than in $\alpha\beta\gamma$ representation, reducing the complexity of modulation algorithm and the computational load associated to it.

A recent survey attributes that 92% of all disturbances in a power system is caused by voltage sags [39]. To solve the voltage sag problem, Dynamic Voltage Restorers (DVR) which include either a 3-phase, 4-wire, 4-leg inverter or a 3-phase, 4-wire, 3-leg inverter(using a split-capacitor configuration) have been used[40]. This involves injecting a voltage through a transformer which is connected in series in order to compensate the voltage drop in the load during a voltage sag condition.

This thesis presents the voltage sag compensator which does not require energy storage devices to provide compensation or mitigation for voltage sags. It is clear from the discussion mentioned that almost all of the solutions are high in cost and are complex, simplified low cost approach intended mainly to provide ride-through for critical loads for voltage sags. The approach can compensate for single-phase sags as well as for poly-phase sags deeper than 50%. The advantages of the proposed approach are:

- Continuous power is maintained to critical loads under voltage sags.
- Do not require energy storage devices.
- Lower cost is achieved due to the use of standard power electronic rectifier, inverter block.
- The system can handle the neutral current under unbalance voltage sags, unbalance load and nonlinear load conditions.

4.2 The System of A 3-Phase 4-Wire 4-Leg Voltage Sags Compensator Based on Three Dimensions Space Vector Modulation in *abc* Coordinates

Fig. 4.1 shows the block diagram of the proposed approach. The system consists of the preferred source, voltage sag detection, controller, full bridge rectifier, boost converter, 3-phase 4-wire 4-leg Inverter that will work as an "alternate supply", main solid state switch (MSSS), auxiliary solid state switch (ASSS) and load.

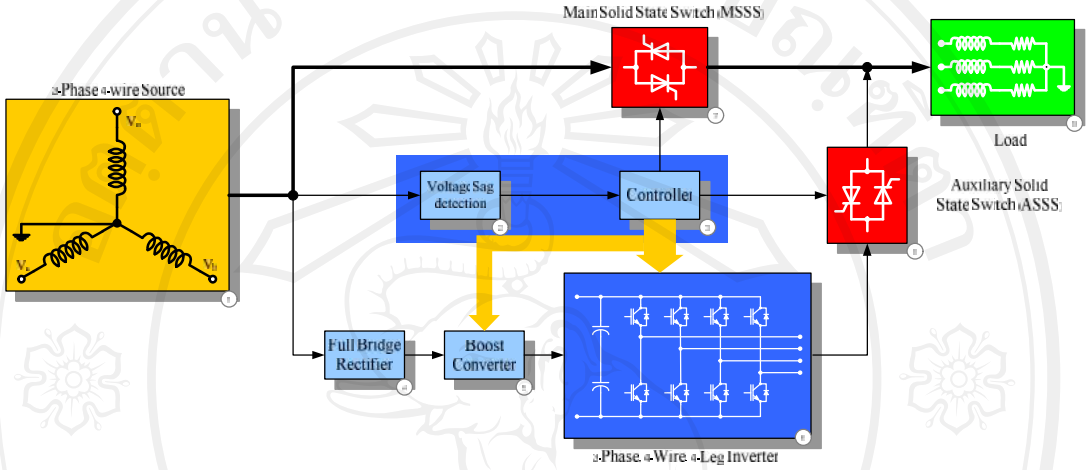

Figure 4.1 Block diagram of 3-phase, 4-wire, 4-leg voltage sag compensator.

Under normal operating conditions, the load is connected to the utility supply via MSSS. In the event of a voltage sag occurrence, the voltage sag detection circuit detects and sends a signal to the controller. The controller turns off the MSSS and then turns on an Auxiliary Solid State Switch (ASSS) whereby transferring the load to the inverter supply. The full wave rectifier converts the utility supply to unregulated DC voltage. Depending upon the voltage sag situation, a boost chopper converts the unregulated DC to a regulated DC link voltage using a boost chopper. The constant DC link voltage is converted by the 3-phase 4-wire 4-leg inverter to a constant AC voltage. This condition is maintained during the entire duration of the voltage sag. Once the utility disturbance is over, the system is reverted to its original operating condition by a sequential turning off the ASSS and turning on of the MSSS. It should be noted that the inverter is continuously operated and its output voltage is properly synchronized with the utility supply voltage.

The controller circuit in Fig. 4.1 is based on dSPic microcontroller which continuously monitors the preferred source voltage to detect for disturbances. The purpose of the control algorithm is to detect out of tolerance conditions and determine the transfer of the critical load to the inverter supply. Further, the function of the dSPic is also to maintain and regulate the DC-link voltage of the inverter stage. This is important since during a voltage sag the available utility input is low. In addition, a regulated DC-link voltage guarantees higher quality voltage to the critical load during a disturbance.

Fig. 4.2 shows a detailed circuit topology to the power electronic conversion block. The bridge rectifier stage converts the AC voltages from the utility supply to a DC voltage that is regulated via the boost converter. The DC/AC inverter provides

compensated three-phase four-wire output voltages to the load that are synchronized with the utility.

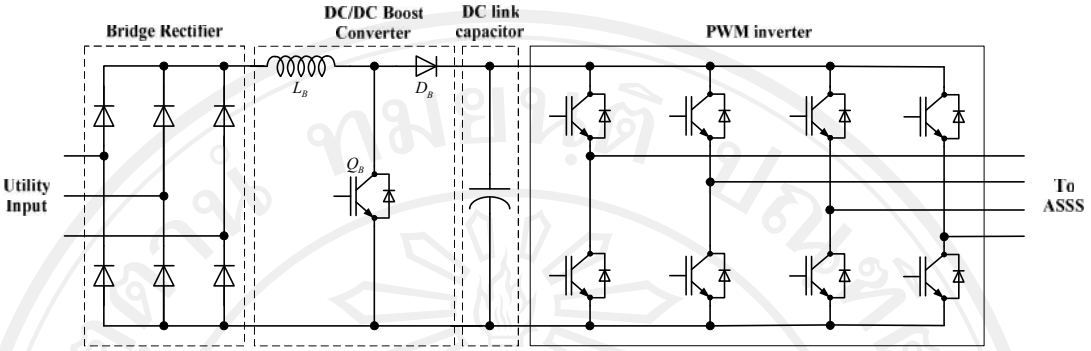

Figure 4.2 Topology of the power electronic conversion block.

4.2.1 Voltage Sag Detection

The voltage sag detector in Fig. 4.1 using opto-isolation amplifier (HCPL-788J) measures 3-phase voltage shown in Fig. 4.4. The core of the voltage sag detection circuit of the controller is the Software Phase-Locked-Loop (SPLL) [40] block diagram shown in Fig. 4.5, which locks a synchronous reference frame (d-q) to the positive sequence component of the utility supply. When the voltage sag occurs in a 3-phase system, it causes voltage unbalance by generating negative and zero sequence voltages. The voltage unbalance causes an oscillation error in the measurement of the phase angle. In Fig. 4.3, the SPLL output, $\hat{\theta}$ is depicted as a nominal unity vector $\hat{V}_{SPLL}$. The phase shift between the actual normalized utility voltage vector $\hat{V}_s$ and the nominal unity vector $\hat{V}_{SPLL}$ can be described in Equation (4.1).

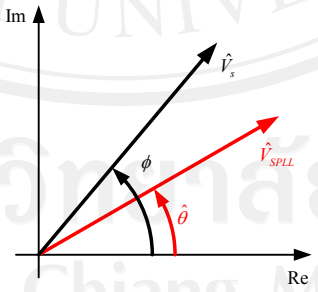

Figure. 4.3 Phase shift of vectors.

This phase shift could be eliminated by using a PI controller of loop filters. Under locked conditions, the argument of the nominal unity vector is equal to the argument of the fundamental positive sequence vector of the utility voltages. The phase voltage V_a, V_b, V_c are obtained from sample line to line voltages are converted into V_α and V_β using Equation (4.2). The transformed voltages are converted into the

Synchronous Rotating Frame (SRF), producing V_d and V_q by using the output angle of the SPLL, $\hat{\theta}$, as shown in (4.3).

$$\phi - \theta = \arctan\left(\frac{V_\beta}{V_\alpha}\right) - \theta \approx \sin(\phi - \theta) = V_\beta \cos\theta - V_\alpha \sin\theta \tag{4.1}$$

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}, \tag{4.2}$$

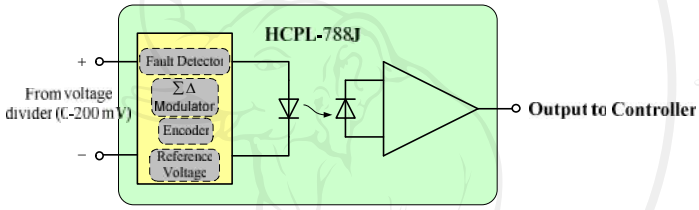

Figure 4.4. Block diagram of opto-isolation amplifier.

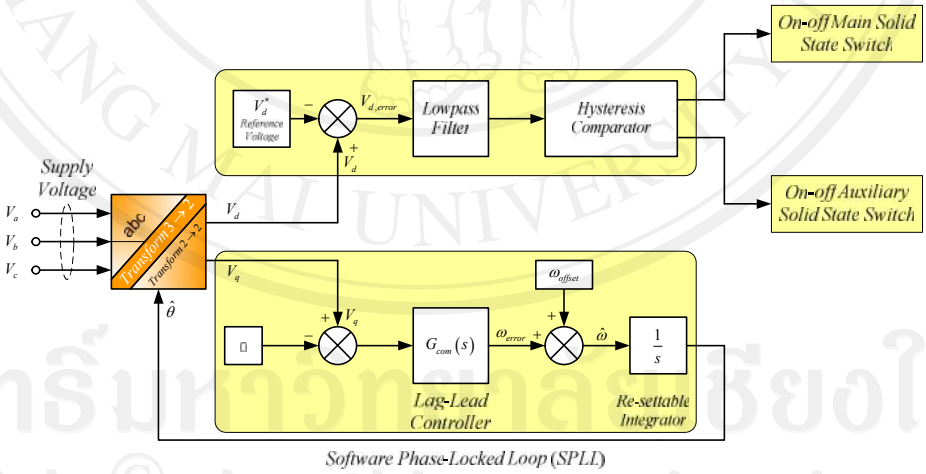

Figure 4.5 Function block diagram of voltage sag detection.

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos(\hat{\theta}) & \sin(\hat{\theta}) \\ -\sin(\hat{\theta}) & \cos(\hat{\theta}) \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix}. \tag{4.3}$$

In order to simplify the control, V_q is normalized using Equation (4.4),

$$V_q = V_\beta \cos\hat{\theta} - V_\alpha \sin\hat{\theta}. \tag{4.4}$$

When the utility voltages are ideal and balanced, the *dq* components of the utility voltage vector, V_s appear as DC values. Therefore, by regulating V_q, it is possible to track accurately the argument of the positive space vector of utility voltages. Typically, a second order feedback control system is implemented for regulating V_q and filtering the higher-order harmonics.

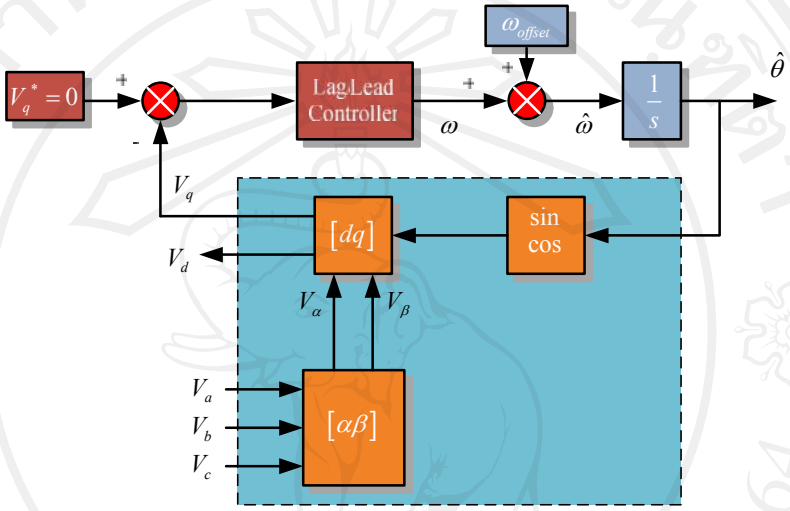

Figure 4.6 Function block diagram of Software Phase-Locked Loop (SPLL).

In the SFR frame, if the output angle $\hat{\theta}$ is identical to the argument of the positive sequence space vector of the utility voltages, then the phase shift is equal to zero. This results in the *dq* components of the utility voltage vector $\hat{V}_s$ to appear as DC values. When the phase shift is small enough, Equation (4.1) becomes valid. The SPLL can thus be treated as a linear control system shown in Fig. 4.7. If G_{con}(s) is a PI controller or a lag/lead controller, the whole SPLL becomes a second-order linear system. A comparison between the characteristics of the PI controller and the lead/lag system will now be made.

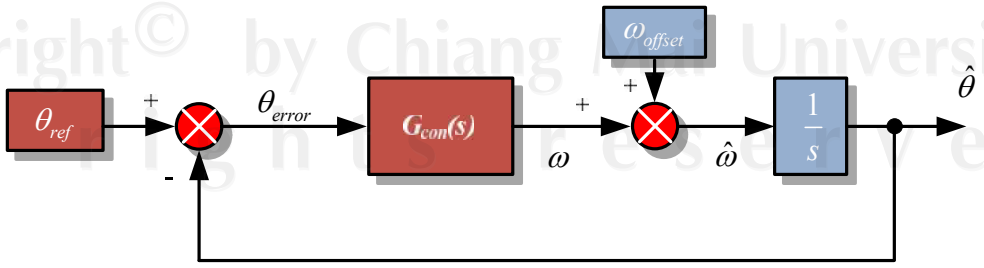

Figure 4.7 Linear model of SPLL.

A. PI controller

For the PI controller, $G_{con}(s)$ can be described as Equation (4.5) and the open and closed loop transfer functions of the SPLL are given in Equation (4.6) and (4.7) respectively,

$$G_{con}(s) = \frac{K_P\left(s + \frac{K_I}{K_P}\right)}{s}, \tag{4.5}$$

$$G_{open}(s) = \frac{K_P\left(s + \frac{K_I}{K_p}\right)}{s^2}, \tag{4.6}$$

$$G_{close}(s) = \left(\frac{K_P s + K_I}{s^2 + K_P s + K_I}\right). \tag{4.7}$$

Let $\xi = \frac{K_P}{2}\cdot\frac{1}{\sqrt{K_I}}$, $\hat{\omega}_n = \sqrt{K_I}$, then

$$G_{close}(s) = \frac{2\xi\hat{\omega}_n s + \hat{\omega}_n^2}{s^2 + 2\xi\hat{\omega}_n s + \hat{\omega}_n^2}.$$

For the controller design, it is desirable to have a good dynamic response and good filtering characteristic. From classical control theory, it is well known that the second-order SPLL system using PI controller has zero steady state error when tracking the step change of θ and ω. However, a steady-state error appears for a step change of the derivative of the frequency. This error could be reduced by increasing the bandwidth. However, a higher bandwidth introduces a large voltage distortion. This results in severe harmonics such as 2nd and 6th order harmonics in the output angle of the SPLL. A trade-off is adopted in practice. Fig. 4.8 shows a bode diagram of the open loop system and Fig. 4.9 shows the root locus diagram of the closed loop system. The chosen parameters are %overshoot < 5%, then: damping raito, $\xi = 0.69$; natural frequency, $\hat{\omega}_n = 20.7\,rad/\sec$, K_P = 28.571, K_I = 428.57 substituting in (4.6) and (4.7). From the bode diagram it is shown that the gain is -26.9 dB and the phase shift is -91.4° when $\hat{\omega} = 628\,\text{rad/s}$.

$$G_{open}(s) = \left(\frac{28.251s + 428.51}{s^2}\right) \tag{4.8}$$

$$G_{close}(s) = \frac{28.251s + 428.51}{s^2 + 28.251s + 428.51} \tag{4.9}$$

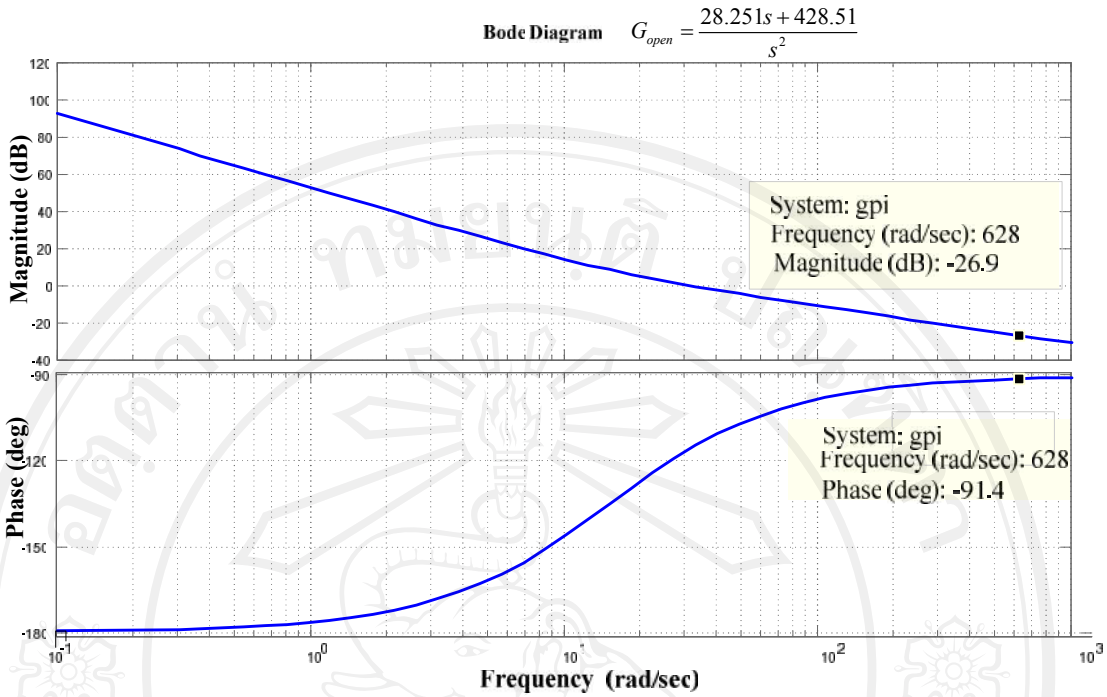

Figure 4.8 Bode diagram of SPLL system using PI controller.

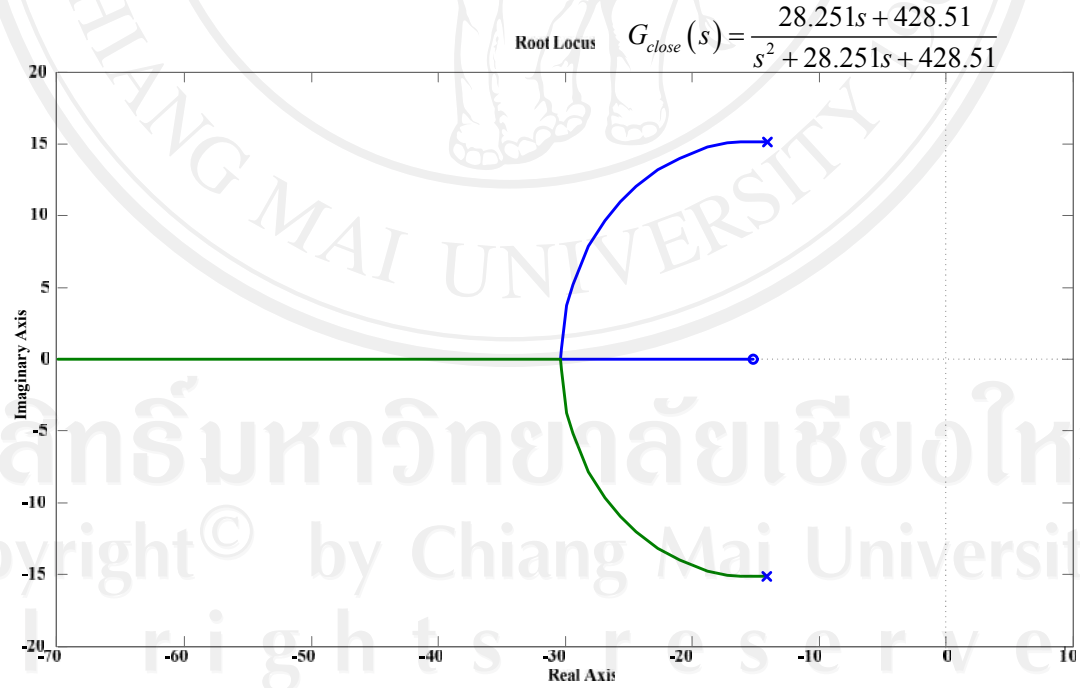

Figure 4.9 Root locus of SPLL system using PI controller.

B. Lag-Lead Controller

The lag-lead controller is modelled by cascade combination of first-order transfer function in the form of $G_{con}(s) = K\dfrac{(1+T_1 s)}{(1+T_2 s)}$. Lag-lead controller is chosen as it exhibits better filtering characteristics. The open loop and the closed loop transfer function of SPLL are given by:

$$G_{open}(s) = \frac{K}{s}\cdot\frac{(1+T_1 s)}{(1+T_2 s)}, \tag{4.10}$$

$$G_{close}(s) = \frac{\left(2\xi\hat{\omega}_n - \dfrac{1}{T_2}\right)s + \hat{\omega}_n^2}{s^2 + 2\xi\hat{\omega}_n s + \hat{\omega}_n^2}, \tag{4.11}$$

where $\xi = \dfrac{1}{2}\cdot\left(\dfrac{KT_1+1}{\sqrt{KT_2}}\right)$; $\hat{\omega}_n = \sqrt{\dfrac{K}{T_2}}$.

The parameters selected are[40] : $\xi = 0.707; \hat{\omega}_n = 31.415\,\text{rad/s}$; $K = 22.85$ and $T_1 = 0.001242; T_2 = 0.02315$.

then $$G_{open}(s) = \frac{1.23s + 987.04}{s^2 + 43.196s},$$

and $$G_{close}(s) = \frac{1.23s + 987.04}{s^2 + 42.43s + 987.04}$$

The parameter of this controller is to filter the 100 Hz and the 300 Hz harmonics and to ensure robustness against the sampling delay time. To meet the first objective T_1 and T_2 are tuned to have and attenuation of $-50\,\text{dB}$ at $2\hat{\omega}_n = 628\,\text{rad/s}$ point with about $-40\,\text{dB/decade}$. Fig. 4.10 shows the bode diagram of the open loop system and Fig. 4.11 had shown the root locus diagram of the closed loop system. The bode diagram shows a gain of $-50\,\text{dB}$ and phase shift of $-139°$ when $\hat{\omega}_n = 628.3\,\text{rad/s}$. A gain of $-60\,\text{dB}$ is observed when $\hat{\omega}_n = 3\times 628.3\,\text{rad/s}$. Therefore, a lag-lead controller has better filtering characteristic when compared with a PI controller. The thesis had used the lag-lead controller for SPLL algorithm to detect the voltage sag.

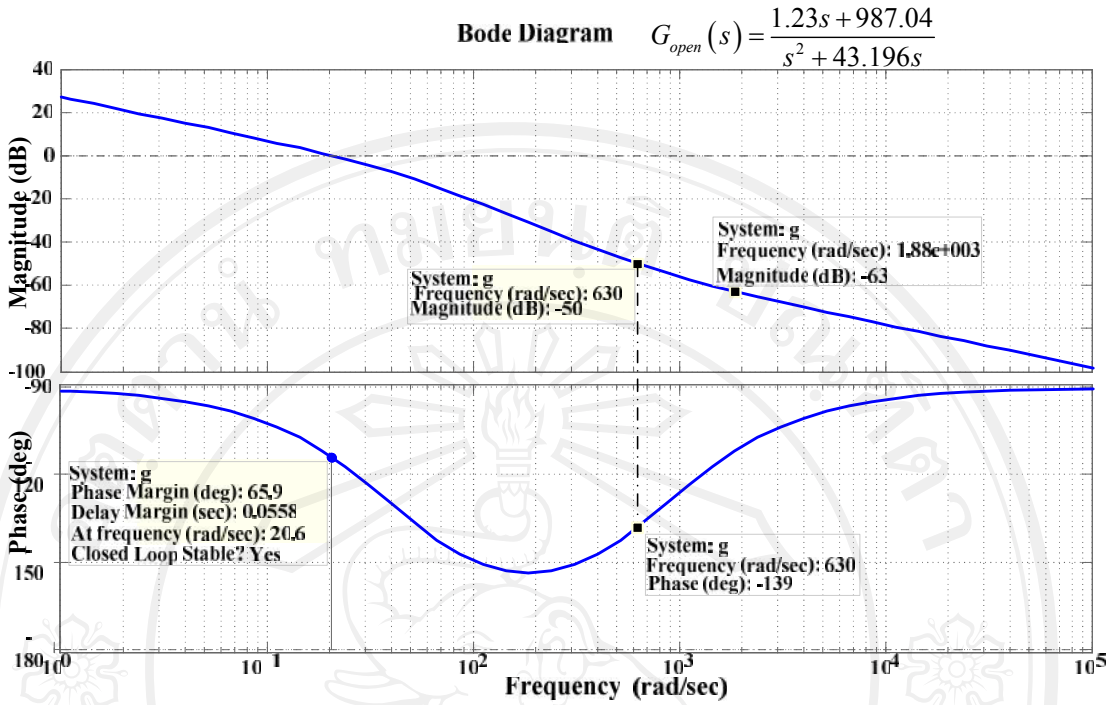

Figure 4.10 Bode diagram of SPLL system using lag-lead controller.

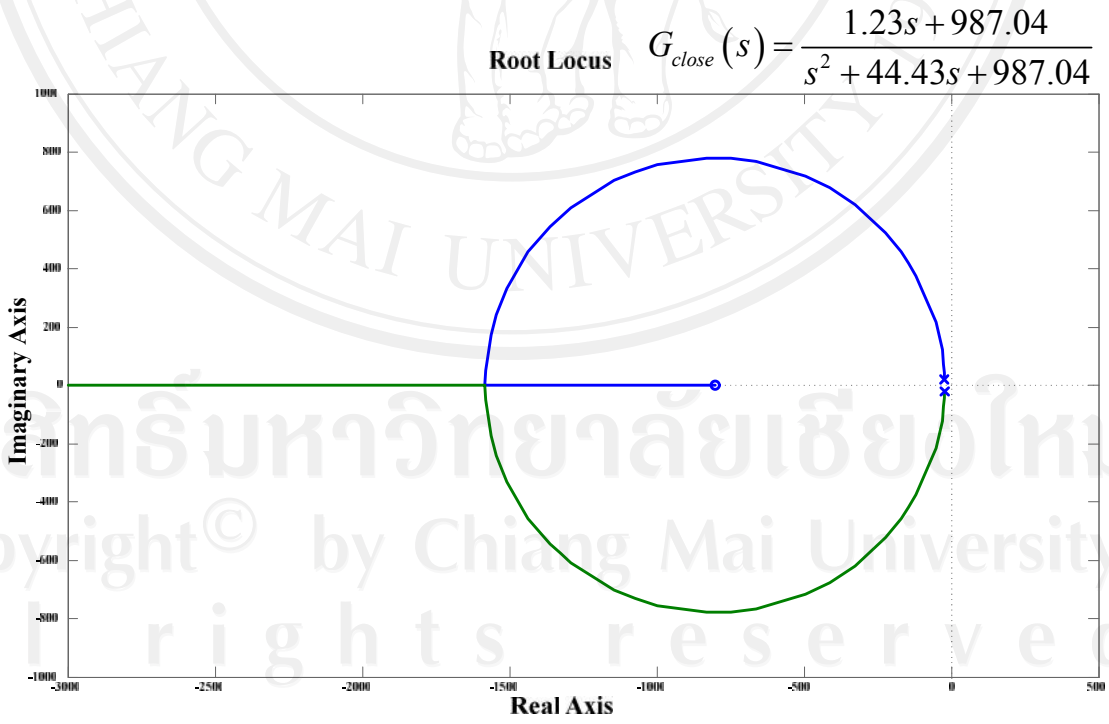

Figure 4.11 Root locus of SPLL system using lag-lead controller.

The construction of voltage sag detector of this thesis was shown in Fig. 4.12.

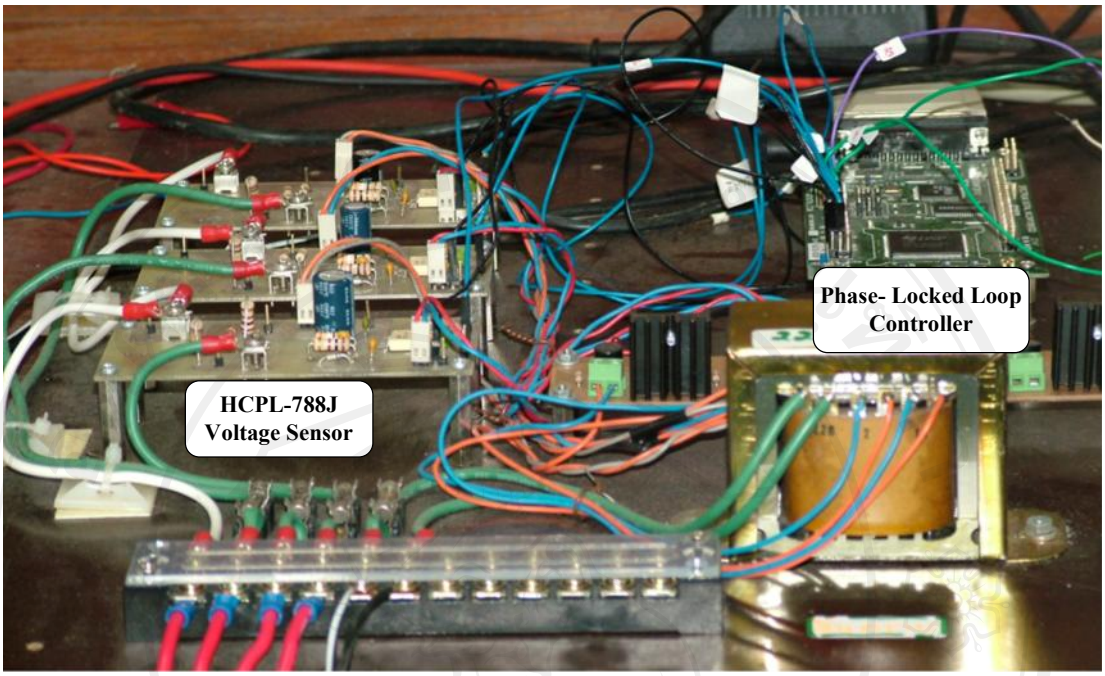

Figure 4.12 The construction of voltage sag dectector of this thesis.

4.2.2 DC/DC Boost Converter

Boost converter is simple, cheap, fast and robust to compensate the DC-link voltage level once a voltage sag in the AC line voltage is detected. Fig. 4.13 is a schematic diagram of the proposed voltage sag detection and compensation.

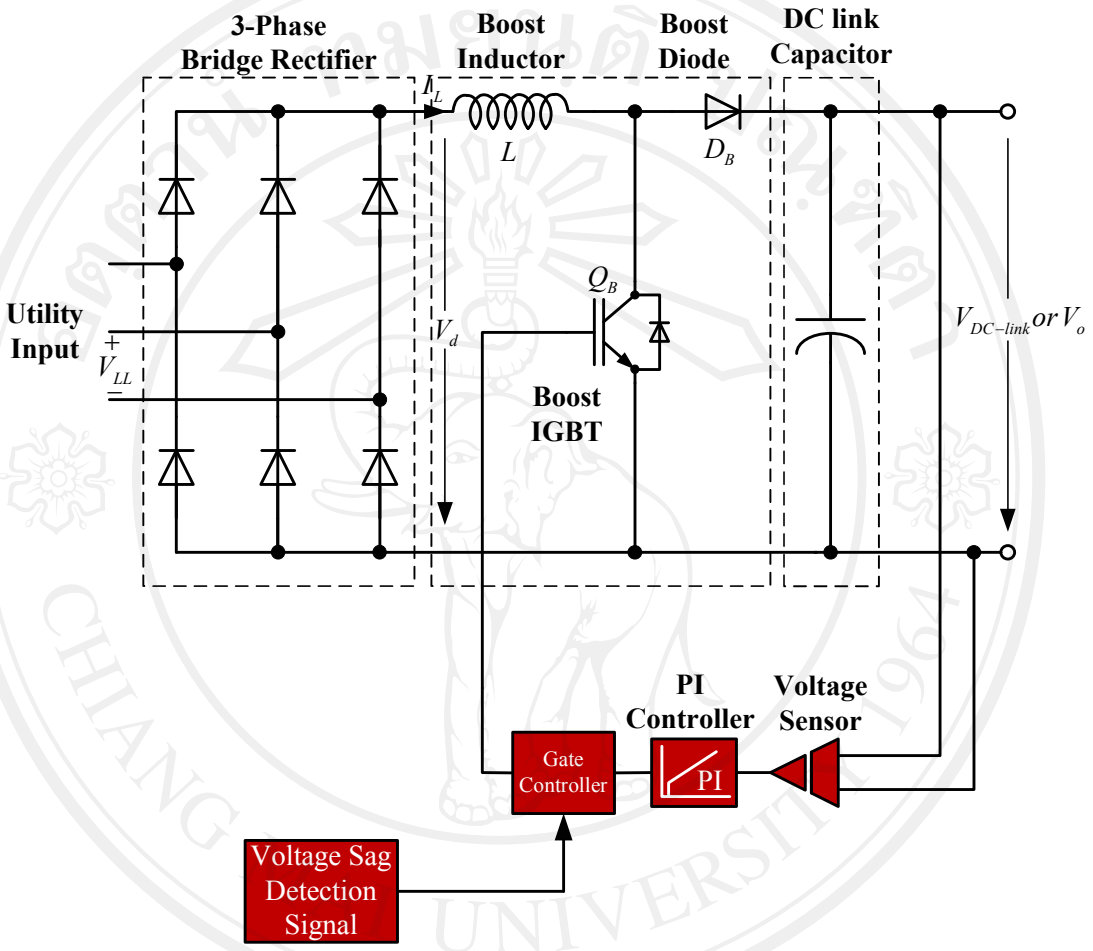

Figure 4.13 DC/DC boost converter in this thesis.

The operation of DC/DC boost converter rectification stage: at which the AC power is converted into DC power using a rectifier circuit; commonly it is a simple 3-leg bridge. The average value of the rectified voltage (in case of 3-phase full wave rectifier) is given by the following formula:

$$V_{DC-link} = 1.35 \times V_{LL}, \quad (4.12)$$

where $V_{DC-link}$ is the DC voltage value at the output of DC/DC boost converter.

V_{LL} is the RMS line-line voltage of the AC supply.

As it is well known that for the boost converter operation in continuous-conduction mode(refer to Fig. 4.14), the relation between the boost converter output voltage $V_{DC-link}$ and the voltage V_d (the boost converter input voltage) in the steady state operation can be controlled by controlling the switching duty cycle of the switch Q_B according to Equation (4.13).

$$\frac{V_{DC-link}}{V_d} = \frac{T_s}{t_{off}} = \frac{1}{1-D}, \tag{4.13}$$

where T_s is the periodic time of a switching cycle.

t_{off} is the duration of the off switching state.

D is the duty cycle.

And according the energy conservation law; assuming lossless circuit, it can be found that

$$\frac{I_o}{I_d} = (1-D), \tag{4.14}$$

Where I_o is the converter output current.

I_d is the input current.

From Equation (4.13), if V_o is set at the desired set point V_o^* while V_d is measured, the switching duty cycle can be calculated according to Equation (4.15) as

$$D = 1 - \frac{V_d}{V_o^*} \tag{4.15}$$

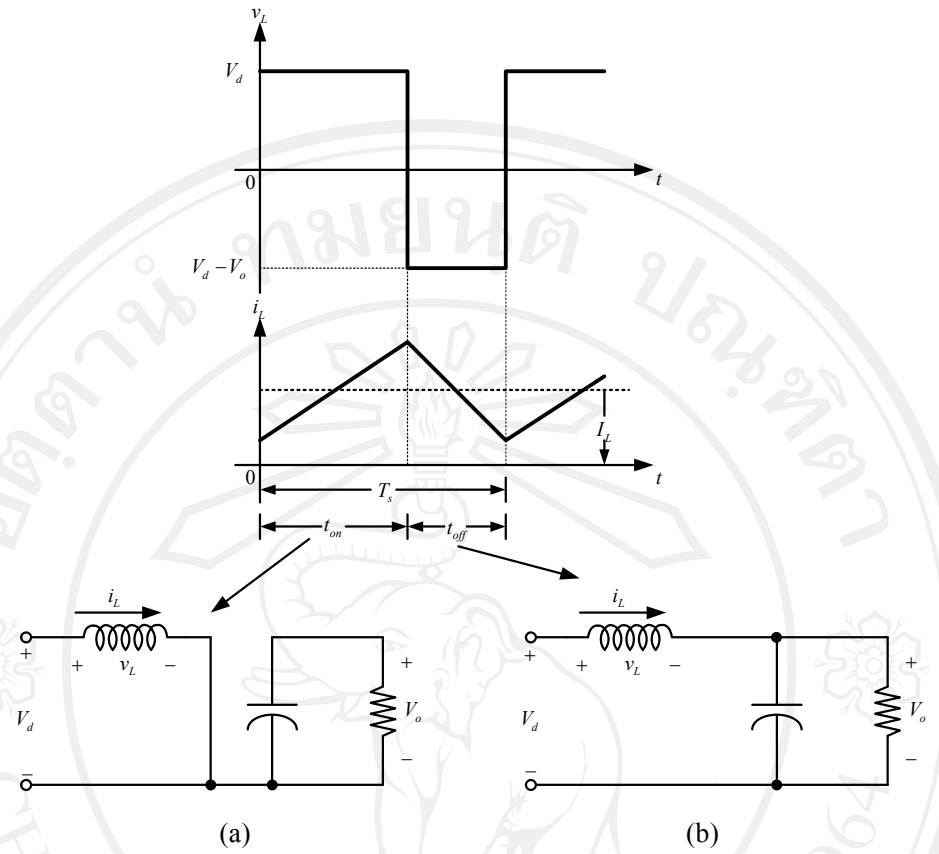

Figure 4.14 Continuous-conduction mode
(a) switch on (b) switch off

It is obvious from this equation that, as long as V_d equals to V_o^* (i.e. when there is no voltage sag), the duty cycle will be zero, which means the supply voltage will be transmitted as is to the inverter. In other words, the boost converter will not be working. The maximum allowable duty cycle is chosen to be 0.5 (i.e. when the voltage sag is 50%) for the sake of preventing I_d of not exceeding double of its rated value during normal operation according to Equation (4.3) (the rated value of I_o is known considered constant as long as the voltage and the load power are considered constant). Thus, the boost converter devices (mainly the inductor L, would be designed to withstand double of the rated DC-Link current I_o).

A design of boost converter simplification is presented in Fig. 4.15 for purposes of designing the elements involved in the converter.

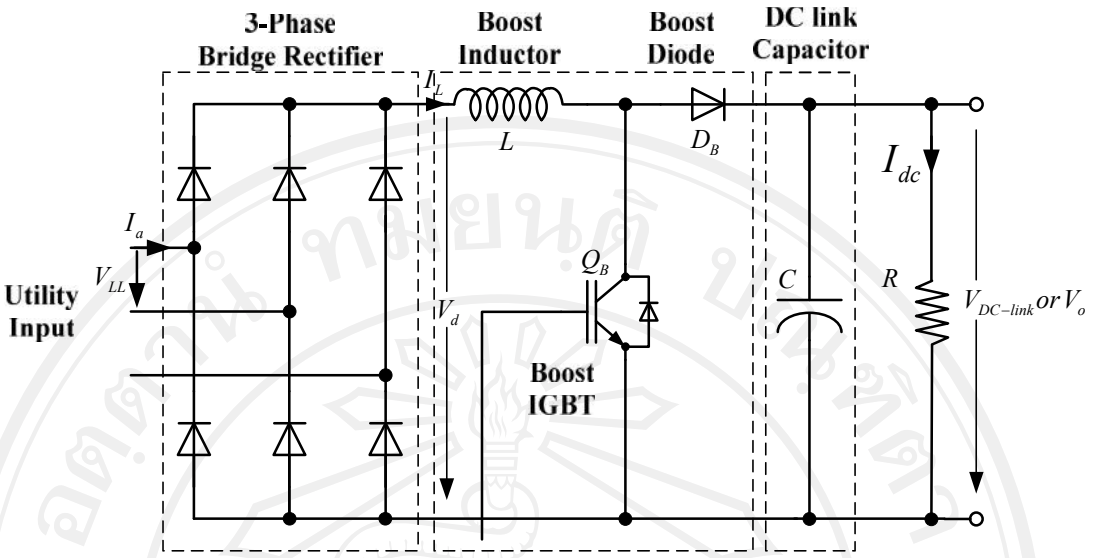

Figure 4.15 The boost converter circuit.

The design is performed for the conditions presented below.

1. Utility rms voltage: $V_{LL} = \sqrt{3} \times 220 = 381.05$ V

2. DC-Link voltage: $V_d = 1.35 \times V_{LL} = 1.35 \times 381.05 = 514.42$ V

3. Output Voltage: $V_o = 600$ V

4. Output power: $P_o = 3$ kVA

5. Load resistor: $R = \frac{V_o^2}{P_o} = \frac{(600)^2}{3000} = 120\,\Omega$

6. Switching frequency: $f_s = 3$ kHz

7. The output DC current is calculated as

$$I_{dc} = \frac{P_o}{V_o} = \frac{3\,kVA}{600} = 5\,\text{A}$$

8. The input AC current is obtained as follows

$$I_a = \sqrt{\frac{2}{3}} I_{dc} = \sqrt{\frac{2}{3}} \times 5 = 2.87\,\text{A}$$

assuming $$I_{L,peak} = 2 \times I_a = 2 \times 2.87\,A = 5.74\,\text{A}$$

Considering the maximum voltage sag of 60%, the required compensation is determined from the following expression

$$\frac{V_o}{V_d} = \frac{1}{1-D}, \tag{4.16}$$

yielding in $$D = 0.4$$

The value of the inductance L_B is computed using the following expression.

$$L_B = \frac{\sqrt{2} \times V_{LL,sag} \times D}{f_s \times I_{L,peak}} = \frac{\sqrt{2} \times 152.42 \times 0.4}{3 \times 10^3 \times 5.74} = 500.71\mu\text{H} \tag{4.17}$$

In this thesis, the $403\,\mu$H boost inductor had constructed and had been using in the boost converter.

The transfer function of the boost converter, assuming constant load and continuous conduction, is given by

$$G_B(s) = \frac{V_o(s)}{V_d(s)} = \frac{\dfrac{V_d}{RC(1-D)^2}\left[\dfrac{R(1-D)^2}{L} - s\right]}{s^2 + \dfrac{1}{RC}s + \dfrac{(1-D)^2}{LC}} \tag{4.18}$$

where: $R = 120\,\Omega, L = 403\,\mu H, C = 470\,\mu F$ and $0.1 < D < 0.4$ for compensation of voltage sags ranging from 10% to 60%. That is, voltage sags less than 10% will not compensated. Equation (4.18) yields:

$$G_B(s) = \frac{34,722.22(107,196.03 - s)}{s^2 + 20.83s + 2,233,250.62} \quad \text{for } D = 0.4 \tag{4.19}$$

$$G_B(s) = \frac{15,432.1(241,191.1 - s)}{s^2 + 20.83s + 5,024,813.9} \quad \text{for } D = 0.1 \tag{4.20}$$

The boost converter is analyzed according the scheme presented in Fig. 4.16.

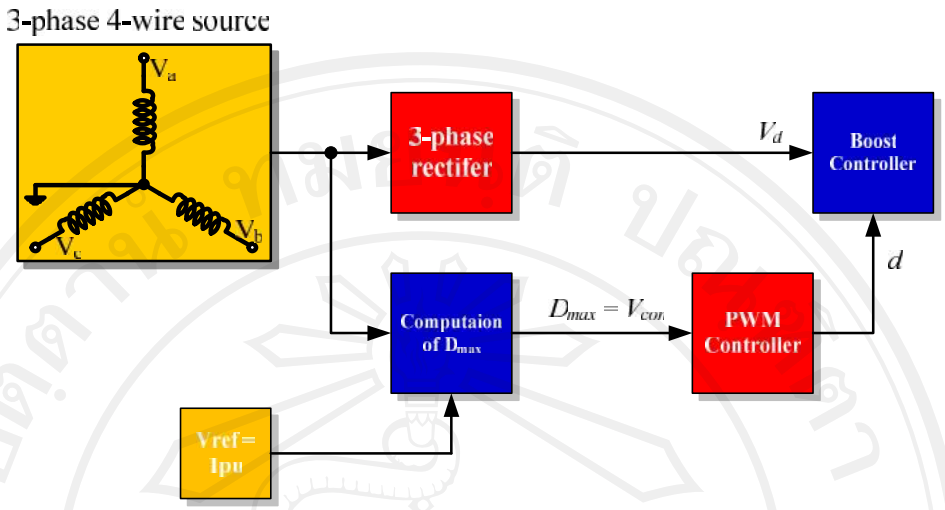

Figure 4.16 Control system of boost converter.

The transfer function for the PWM controller is obtained in (4.21) as

$$T_m(s) = \frac{V_d(s)}{V_{con}(s)} = 0.2, \tag{4.21}$$

There, the transfer function composed by the converter plus its PWM controller is defined as

$$T_1(s) = T_m(s) \times G_B(s), \tag{4.22}$$

Yielding in

$$G_{B\_04}(s) = \frac{744,416,825.81 - 6,944.44s}{s^2 + 20.83s + 2,233,250.62} \quad \text{for } D = 0.4 \tag{4.23}$$

and

$$G_{B\_01}(s) = \frac{744,417,034.7 - 3,086.42s}{s^2 + 20.83s + 5,024,813.9} \quad \text{for } D = 0.1 \tag{4.24}$$

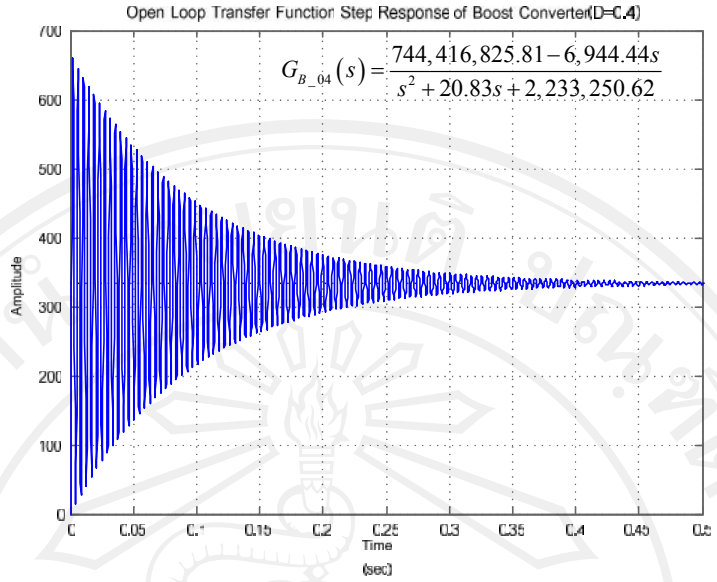

Figure 4.17 Step response of boost converter (D=0.4).

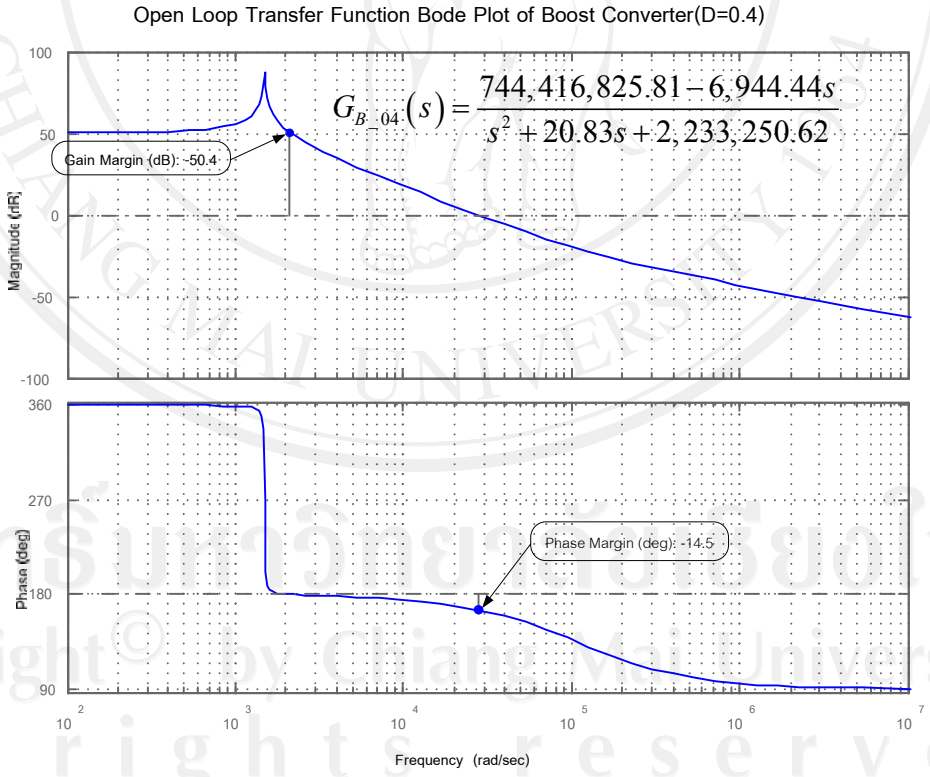

Figure 4.18 Bode plot of boost converter (D=0.4).

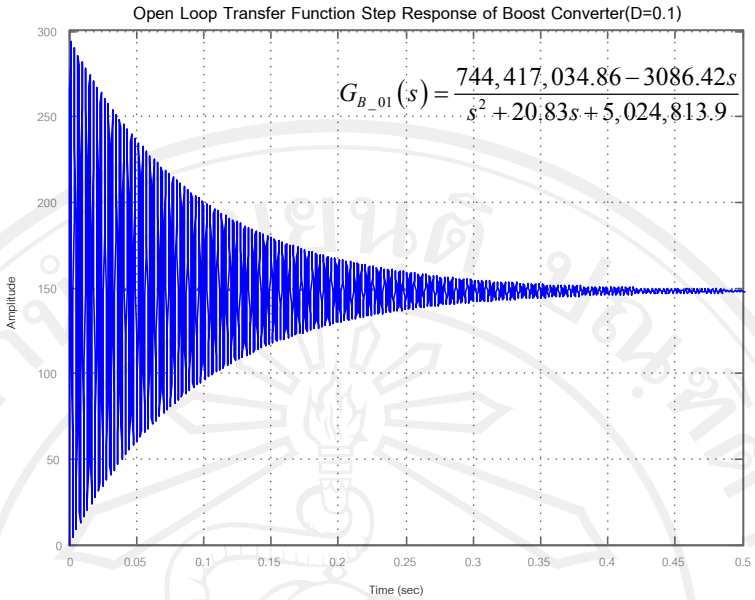

Figure 4.19 Step response of boost converter (D=0.1).

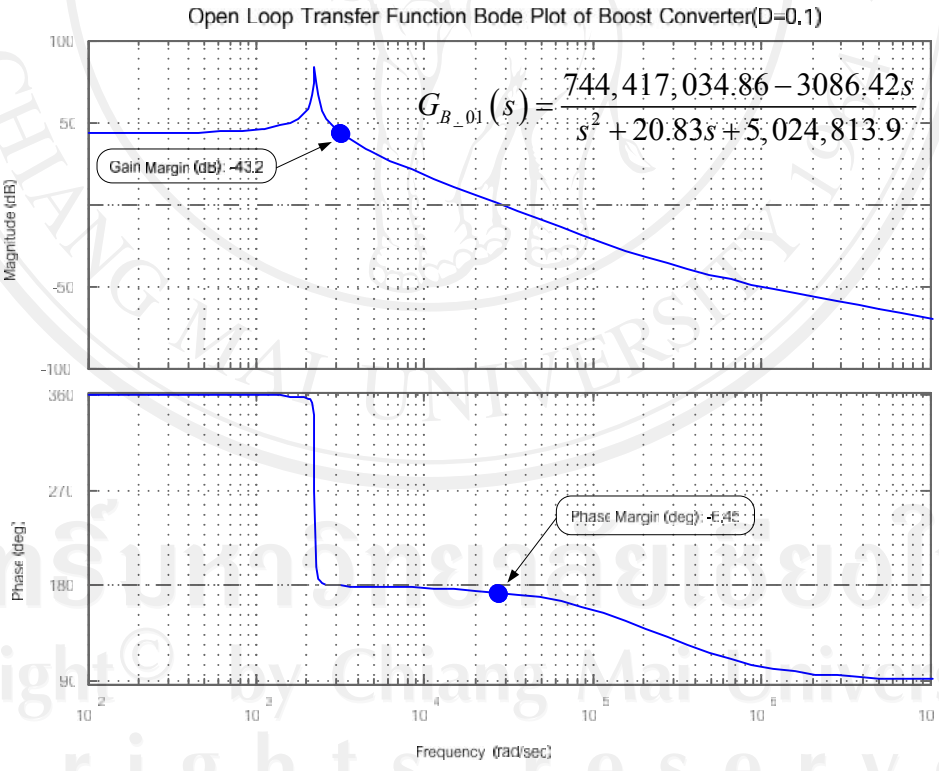

Figure 4.20 Bode plot of boost converter (D=0.1).

Used SISOTOOL in MATLAB to auto-tunning PI controller:
D = 0.4 from auto-tunning

$$PI_{04}(s) = \frac{-0.00012784s + 0.031181}{s} \tag{4.25}$$

and

D = 0.1 from autotunning

$$PI_{01}(s) = \frac{0.31334 \times 10^{-6} s + 0.10805}{s} \tag{4.26}$$

Closed loop transfer function of boost converter

D = 0.4

$$G_{B\_PI\_04}(s) = \frac{0.8878s^2 - 0.938 \times 10^4 s + 2.32 \times 10^6}{s^3 + 20.83s^2 + 2.223 \times 10^6 s}$$

D = 0.1

$$G_{B\_PI\_01}(s) = \frac{-0.0009671s^2 - 100.2s + 8.04 \times 10^4}{s^3 + 20.83s^2 + 5.025 \times 10^6 s}$$

The step response and bode response of closed loop transfer function and PI controller are shown in Fig.4.21 to Fig.4.24

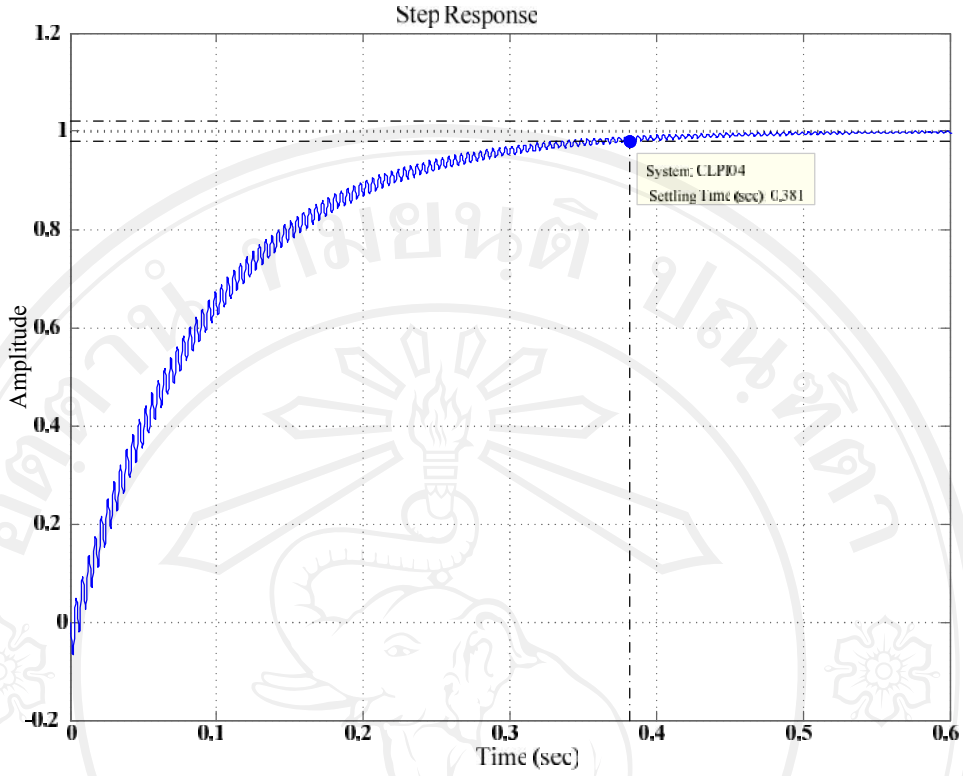

Figure 4.21 Step response of boost converter (D=0.4) with PI control.

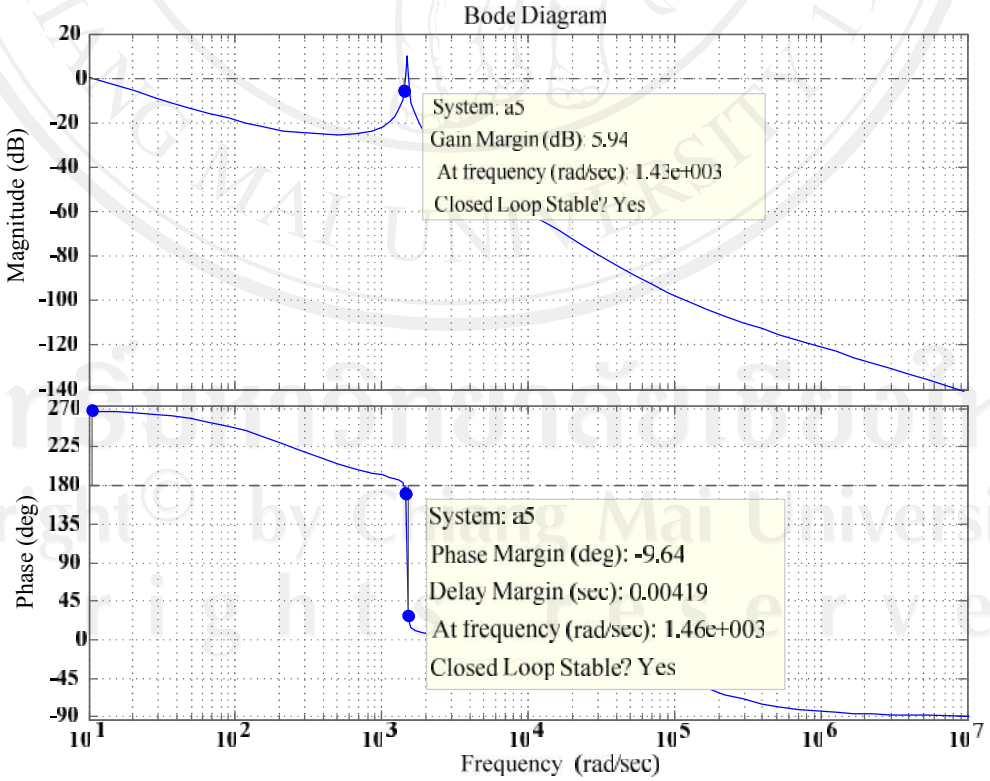

Figure. 4.22 Bode plot of boost converter (D=0.4) with PI control.

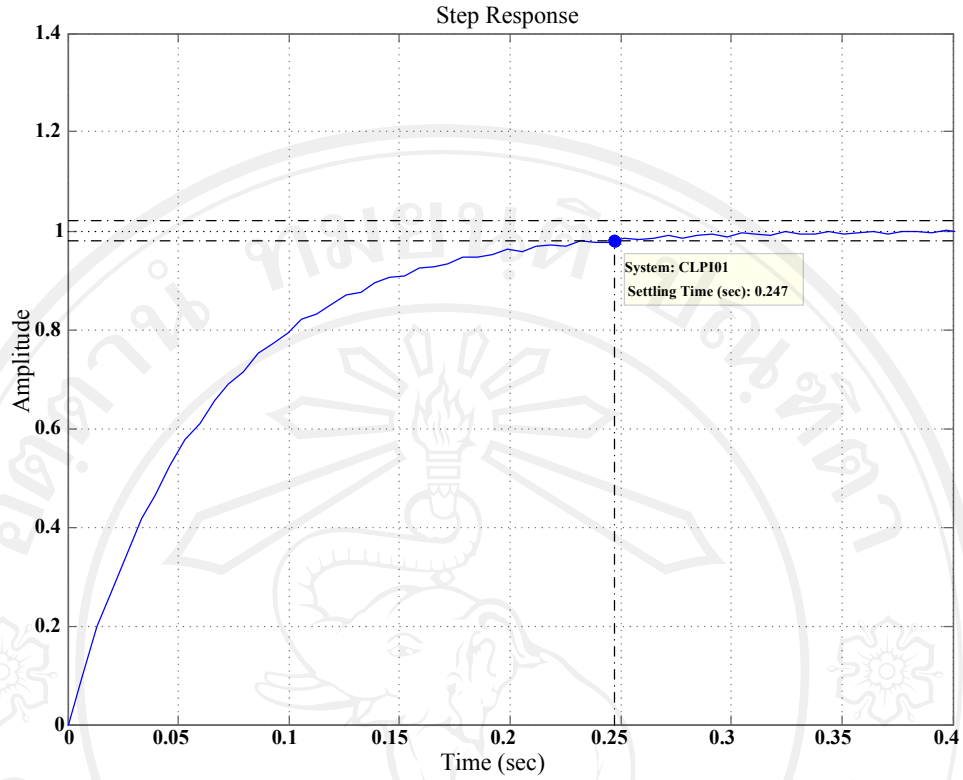

Figure. 4.23 Step response of boost converter (D=0.1) with PI control.

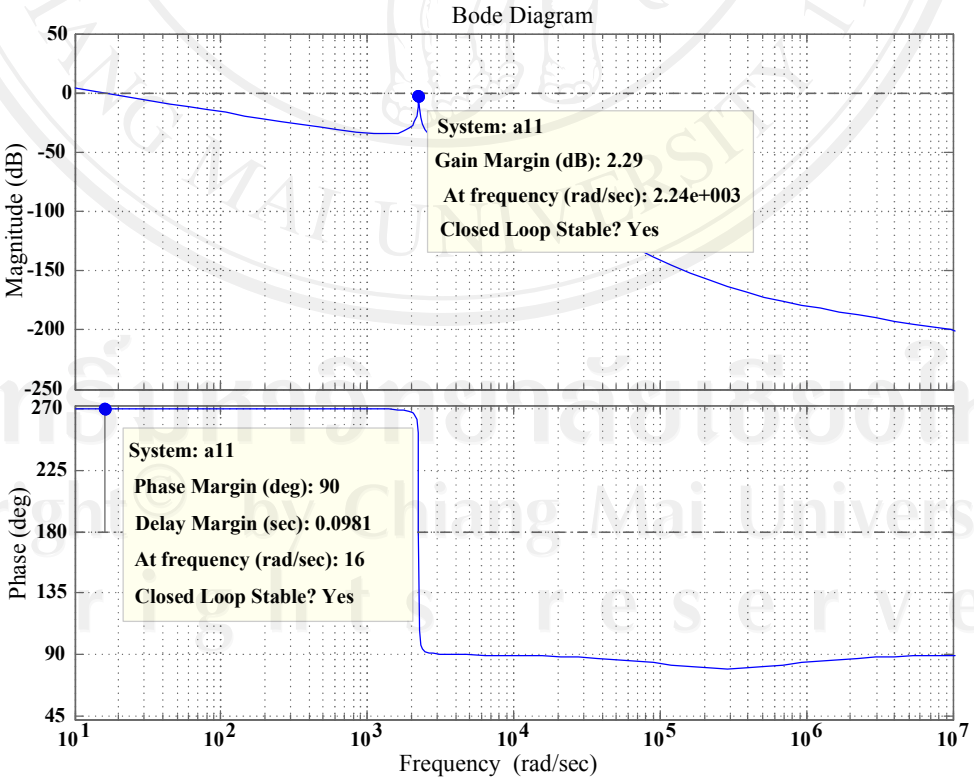

Figure 4.24 Bode plot of boost converter (D=0.1) with PI control.

The continuous time domain is then transformed to the z-plane and the controller designed in the z-plane. Equation (4.27) and (4.28) are the PI controller continuous time domain, the PI algorithm has general form: [41]

$$u(t) = K_p e(t) + \frac{K_p}{T_i}\int_0^t e(t)\,dt, \tag{4.27}$$

where: $e(t)$ is the error signal,
$u(t)$ is the control input to the process,
K_p is proportional gain,
T_i is the integral time constant,

In s-domain, the PI controller can be written as:

$$U(s) = K_p\left[1 + \frac{1}{T_i s}\right]E(s) \tag{4.28}$$

The discrete form of the PI controller can be derived by finding the z-transform of Equation (4.28) :

$$U(z) = E(z)K_p\left[1 + \frac{T_s}{T_i\left(1 - z^{-1}\right)}\right] \tag{4.29}$$

where: T_s is the sampling time

Rewriting Equation (4.29) as,

$$\frac{U(z)}{E(z)} = a + \frac{b}{\left(1 - z^{-1}\right)} \tag{4.30}$$

where: $a = K_p$

$$b = \frac{K_p T_s}{T_i}$$

From Equation (4.25): if $T_s = 0.33333\times10^{-6}$ s then from

$$PI_{04}(s) = 0.031181\times\frac{(1-0.0041s)}{s}$$

or $$PI_{04}(s) = 127.841\times10^{-6}\left[-1+\frac{1}{0.0041s}\right]$$

then: $$a = -127.841\times10^{-6}$$

$$b = \frac{127.841\times10^{-6}\times0.33333\times10^{-6}}{0.0041} = 1.04\times10^{-8}$$

From Equation (4.26)

$$PI_{01}(s) = 0.10805\times\frac{(1-2.9\times10^{-6}s)}{s}$$

or $$PI_{01}(s) = 0.313345\times10^{-6}\left[-1+\frac{1}{2.9\times10^{-6}s}\right]$$

then: $$a = -0.313345\times10^{-6}$$

$$b = \frac{0.313345\times10^{-6}\times0.33333\times10^{-6}}{2.9\times10^{-6}} = 3.61\times10^{-8}$$

The practical problem when the standard form of the PI controller is used is known as the *"integral windup"* which can cause long periods of overshoot in the controller response. The PI controller in Fig. 4.25 shows the practice realization of the PI controller to solve this problem.

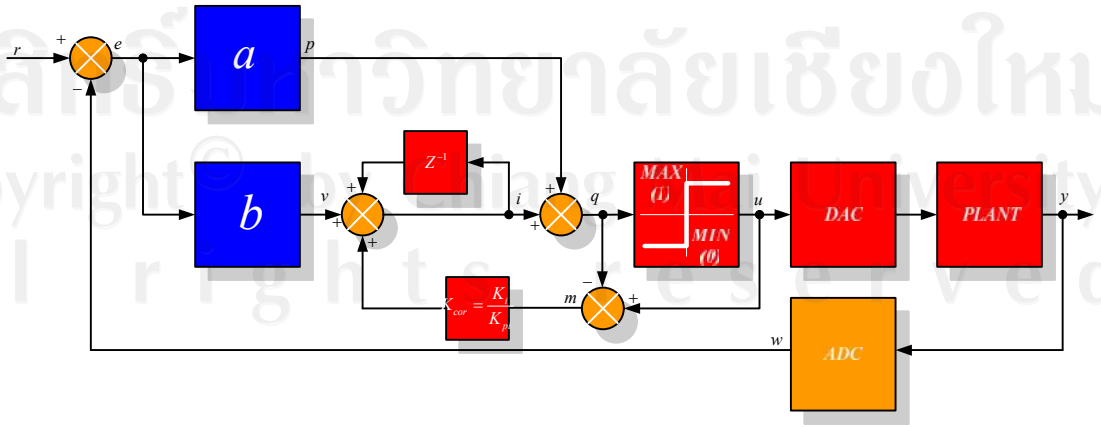

Figure 4.25 The practical realization of the PI controller.

The algorithm of PI controller in Fig. 4.24 can be written as:

BEGIN

DO FOREVER

Get set point: $r(kT_s)$

Get system output: $w(kT_s)$

Calculate error: $e(kT_s) = r(kT_s) - w(kT_s)$

Calculate P term: $p(kT_s) = a \times e(kT_s) + p(kT_s - T_s)$

$v(kT_s) = b \times e(kT_s) + v(kT_s - T_s)$

Calculate I term: $i(kT_s) = v(kT_s) + K_{cor} \times m(kT_s) + i(kT_s)$

Calculate PI term: $q(kT_s) = i(kT_s) + p(kT_s)$

$u(kT_s) = q(kT_s)$

$m(kT_s) = u(kT_s) - q(kT_s)$

IF $u(kT_s) > MAX$

$u(kT_s) = q(kT_s)$

ELSE IF $u(kT_s) < MIN$

$u(kT_s) = q(kT_s)$

END IF

Send control to actuator

Save variable: $u(kT_s - T_s) = u(kT_s)$

$w(kT_s - T_s) = w(kT_s)$

Wait for next sample

ENDDO

END

The prototype of DC/DC converter in this thesis was shown in Fig. 4.26

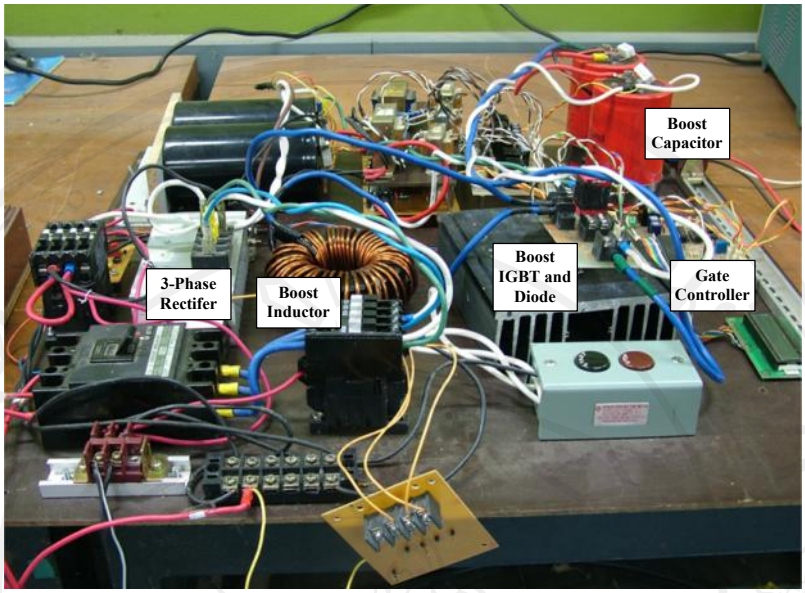

Figure 4.26 The DC/DC boost converter of this thesis.

4.2.3 Solid State Transfer Switch

From the block diagram in Fig.4.1, the solid state transfer switch consists of Main Solid State Switch (MSSS) and Auxiliary Solid State Switch (ASSS). The block diagram of solid state transfer switch is shown in Fig. 4.27.

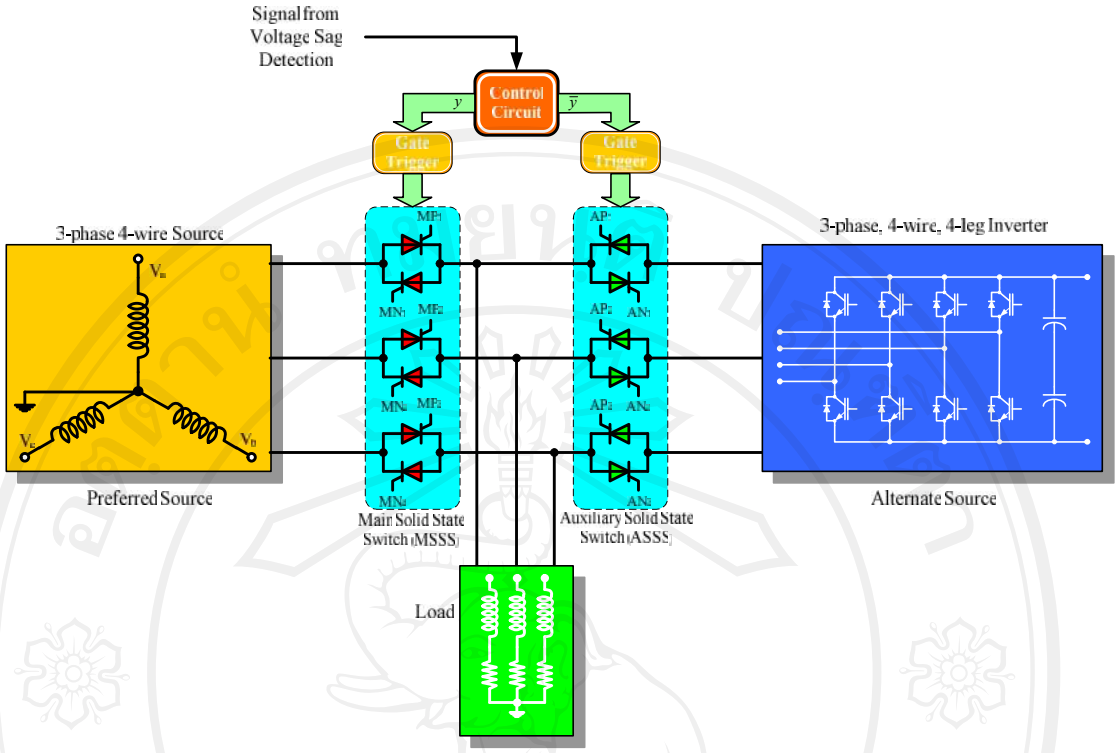

Figure 4.27 The block diagram of solid state transfer switch.

The solid state transfer switch MSSS and ASSS consist of three thyristor modules corresponding to three phases of the system. In each thyristor module, two sets of the SCR switches are connected in anti-parallel allowing the current to flow in both positive and negative directions.

The switching of the solid state transfer switch can be divided into two sections,

1) steady state switching

- Under normal operating conditions, the load is connected to the preferred source via MSSS 'on' $(y = '1')$ and ASSS 'off' $(\overline{y} = '0')$.
- Under voltage sag conditions, the load is connected to alternate source via ASSS 'on' $(\overline{y} = '1')$ and MSSS 'off' $(y = '0')$.

2) transfer switching

The transfer signal is a logic signal from voltage sag detector circuit that selects which the source for the load. It transfers the load from the preferred source to alternate source when voltage sag occurs and transfers back when voltage sag is over.

- When the voltage sag occurs at the preferred source side, the load is transferred to the alternate source by voltage sag detection signal to change signal $y = '1'$ to $y = '0'$ (transition y from $'1' \rightarrow '0'$ MSSS 'off' state) and signal $\overline{y} = '0'$ to $\overline{y} = '1'$(transition $\overline{y}$ from $'0' \rightarrow '1'$ ASSS 'on' state).

- When the preferred source is back to normal conditions, the load is transferred back from the alternate source to the preferred source by voltage sag detection signal to changed signal $y = '0'$ to $y = '1'$ (transition y from $'0' \rightarrow '1'$MSSS 'on' state) and signal $\overline{y} = '1'$ to $\overline{y} = '0'$ (transition $\overline{y}$ from '1' to '0' ASSS 'off' state).

The operation of solid state transfer switch is shown in Fig. 4.28.

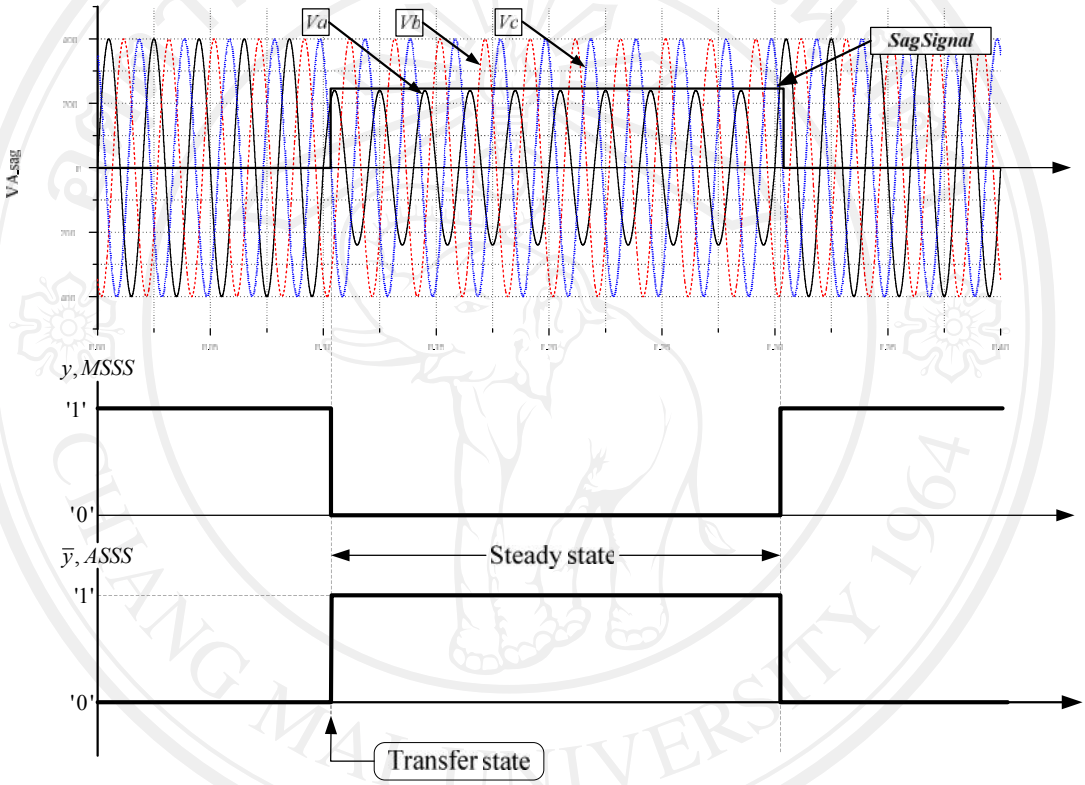

Figure 4.28 The operation of solid state transfer switch.

The gate trigger for SCR is to provide a gate current of the right amplitude, at the right time and of the right duration. Thyristors are current controlled devices and therefore they need drivers that behave like current sources. These drivers need to be isolated from the power circuit for a reliable operation. This is accomplished either by pulse transformers or opto-couplers.

The gate drive circuit of gate trigger used a pulse transformer to couple the trigger pulse to the SCR gate (Fig. 4.29). One gate trigger circuit per SCR was used.

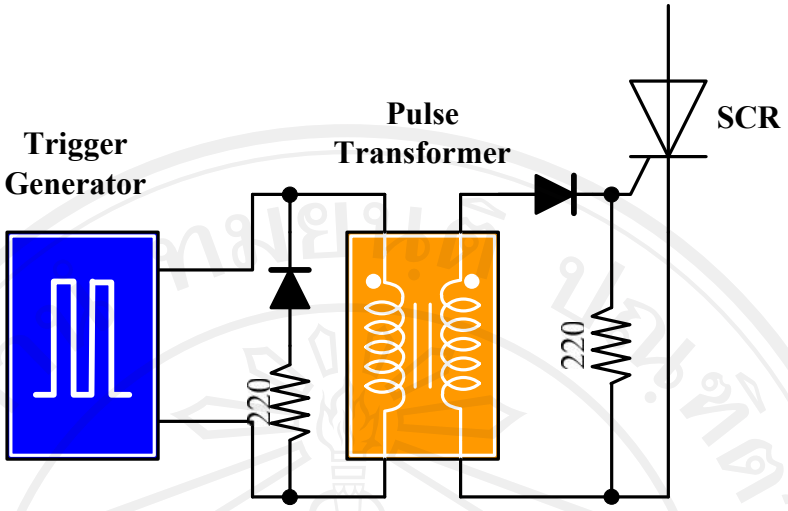

Figure 4.29 Pulse transformer trigger circuit.

The two gate drivers for one SCR module were used. The circuit is shown in Fig. 4.30.

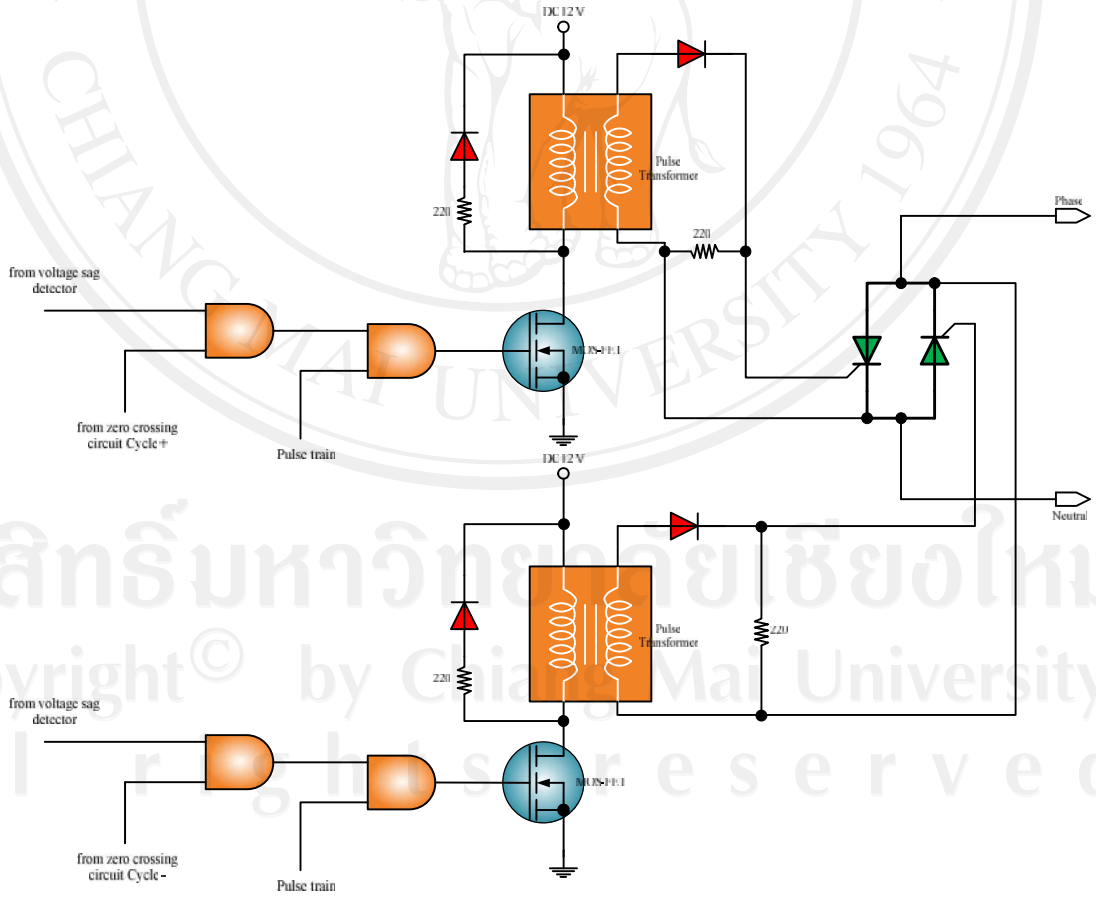

Figure 4.30 The circuit for 1 module of SCR.

The actual of circuit in Fig. 4.30 was shown in Fig. 4.31.

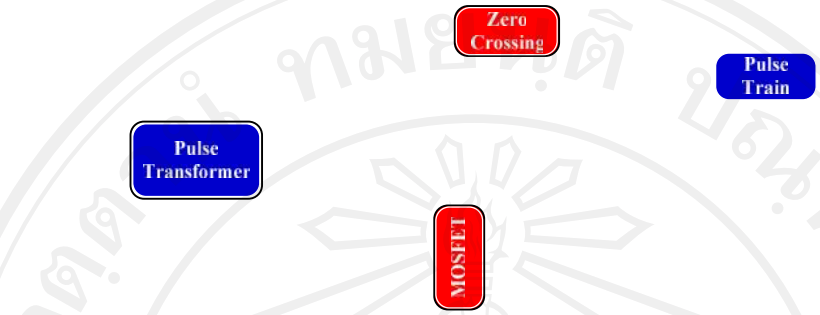

Figure 4.31 The circuit board of trigger circuit.

4.2.4 Four-leg voltage source inverter

In many commercial and industrial applications, the power is distributed through a 3-phase, 4-wire system. It allows to supply on arbitrary loads: unbalanced and/or balanced, linear or nonlinear. In power electronics two alternative methods of forming the output neutral terminal are applied[42].

- DC link splitting using a capacitor voltage divider to form the neutral leg (Fig. 4.31)
- Addition of fourth leg as a neutral terminal to a conventional 3-phase bridge inverter (Fig. 4.34)

4.2.4.1 Split capacitor inverters[43]

Three leg inverters systems have a lot of disadvantages, especially when the load is unbalanced. The demerit of split capacitor inverter is that the large and expensive DC link capacitors are needed to maintain an acceptable voltage ripple level across the DC link capacitors in case of a large zero sequence current due to unbalanced or nonlinear load. The circuit in Fig.4.32 is the VSI (voltage source inverter) for 3-phase 4-wire application. It consist of three half bridges. Each of them supplies a phase of the load circuit. Due to the connection of the star point n with midpoint of the DC link capacitor, three independent half bridge inverters, which share the same DC link voltage, are produced. The switch state s is defined as follows:

$s_x = 1$ when the upper switch is on and the lower one is off

$s_x = -1$ when the upper switch is off and the lower one is on

The current i_{d+} and i_{d-} will flow through the DC link as

$$i_{d+} = \frac{1+s_a}{2} i_a + \frac{1+s_b}{2} i_b + \frac{1+s_c}{2} i_c , \tag{4.31}$$

$$i_{d-} = \frac{1-s_a}{2} i_a + \frac{1-s_b}{2} i_b + \frac{1-s_c}{2} i_c . \tag{4.32}$$

When the load is balanced, the sum of all three phase currents is zero. In this case the same currents will flow through the DC link but with different sign. The DC link currents equations (4.31), (4.32) can be also written as (4.33) and (4.34).

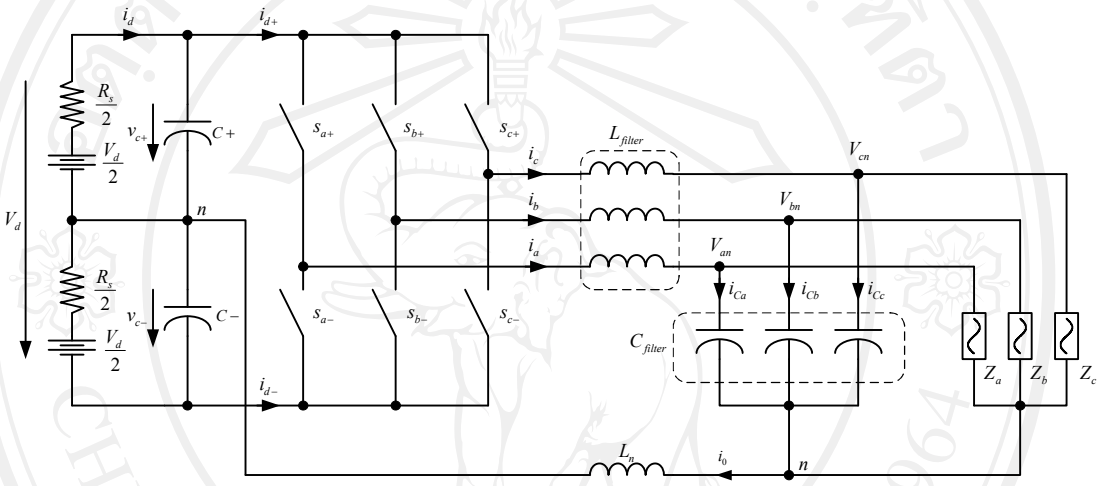

Figure 4.32. Three phases capacitors split inverter.

In this capacitors split inverter, the DC link currents consist of a switching current and zero sequence current.

$$i_{d+} = \frac{\left(s_a i_a + s_b i_b + s_c i_c + 3i_0\right)}{2}, \tag{4.33}$$

$$i_{d-} = -\frac{\left(s_a i_a + s_b i_b + s_c i_c - 3i_0\right)}{2} . \tag{4.34}$$

The DC link voltage of each capacitor is given by

$$v_{c+} = \frac{0.5\left(V_d - R_s i_{d+}\right)}{\left(\frac{sC_+ R_s}{2} + 1\right)} , \tag{4.35}$$

$$v_{c-} = \frac{0.5\left(V_d + R_s i_{d-}\right)}{\left(\frac{sC_- R_s}{2} + 1\right)} , \tag{4.36}$$

when s = Laplace operator
V_d = the battery voltage
R_s = battery resistance.

Disadvantage of the split capacitor inverter is that the zero current flows directly through the DC link capacitor and cause a ripple in the DC link voltage. To reduce this voltage ripple a very high DC link capacitance must be used (Fig.4.33 and Fig.4.34). Another disadvantage is the additional power losses caused by the zero sequence current in DC link capacitor.

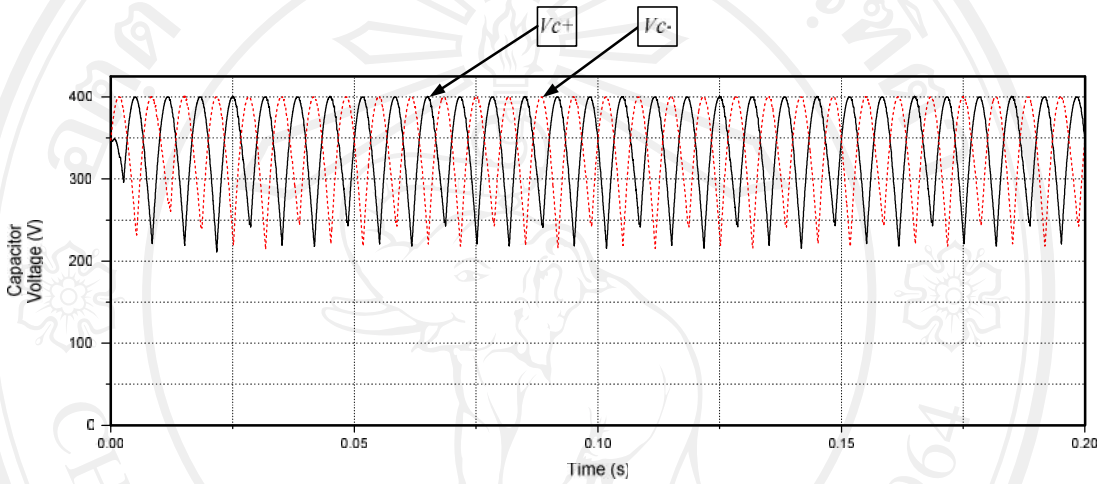

Figure 4.33 DC-link capacitor is 1000 μF .

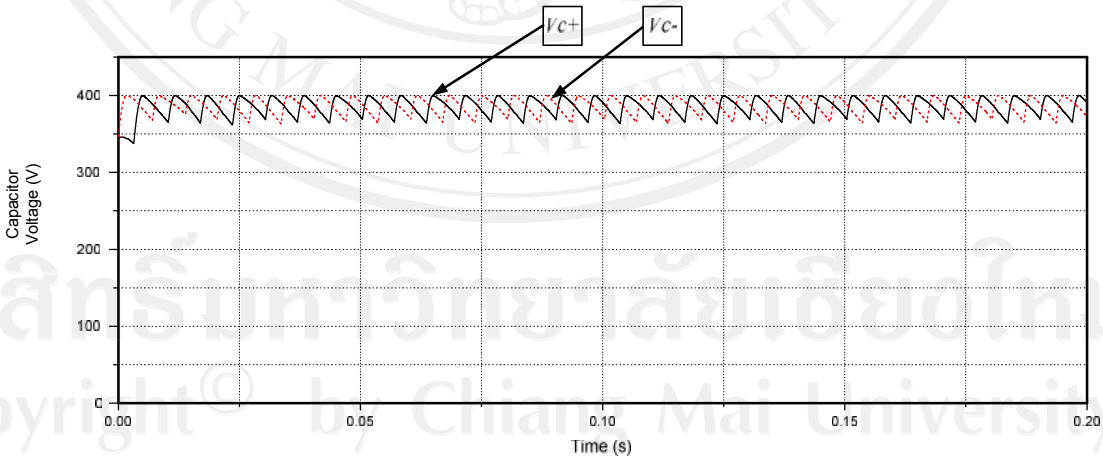

Figure 4.34 DC link capacitor is 10000 μF .

These losses are indirect proportional to the frequency and are maximum at 50 Hz.

4.2.4.2 Four-leg voltage source inverter [50]

The three-phase four-leg inverter is shown in Fig. 4.35. Compared with the split capacitor inverter, the additional fourth leg provides a return path for the load neutral point so that the zero sequence component can be regulated and substantially reduce the DC link capacitor. The neutral inductor L_n can reduce switching frequency ripple.

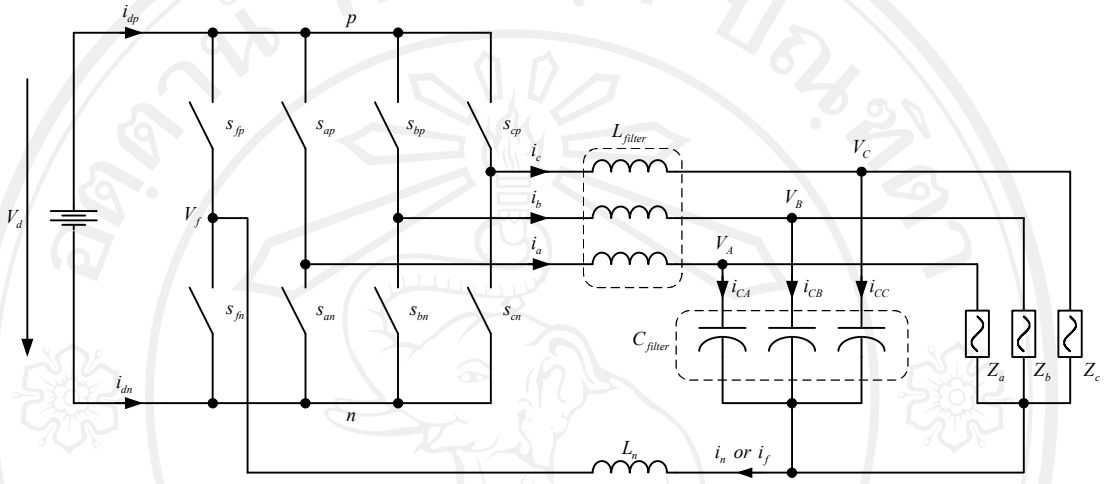

Figure 4.35 Four-leg voltage source inverter

In this case, the star point of the load and output filter is connected to the 4th leg. Depending on the switching state $(s_x = 1 \text{ or } s_x = -1)$ the load underlies either the positive p or negative n potential of the DC link. The current of the DC link capacitor was shown in equation (4.37) and (4.38)

$$i_{dp} = \frac{1+s_a}{2} i_a + \frac{1+s_b}{2} + i_b + \frac{1+s_c}{2} i_c - \frac{1-s_f}{2} i_f \quad , \tag{4.37}$$

$$i_{dn} = -\left(\frac{1-s_a}{2} i_a + \frac{1-s_b}{2} i_c + \frac{1-s_c}{2} i_c - \frac{1-s_f}{2} i_f \right). \tag{4.38}$$

From the equation (4.37) and (4.38) one can see that an additional addend appears in equations. Equation (4.37) and (4.38) can also be written as (4.39) and (4.40). It can be seen, that in this case no zero sequence current flows through the DC link but only switching currents.

$$i_{dp} = \frac{\left(s_a i_a + s_b i_b + s_c i_c - s_f i_f \right)}{2}, \tag{4.39}$$

$$i_{dn} = -\frac{\left(s_a i_a + s_b i_b + s_c i_c - s_f i_f\right)}{2}. \tag{4.40}$$

The advantages of the four-leg inverter in Fig. 4.34 are:

1) higher utilization of the DC link voltage.
2) small DC link capacitor as no zero sequence current flows through the DC link capacitor.
3) additional degree of freedom due to the 4th leg.

4.2.5 The three-dimensional space vector.

There are several types of three-dimensional space vector for four-leg inverter as:

1) three-dimensional space vector in $\alpha\beta\gamma$ coordinates.
2) three-dimensional space vector in *abc* coordinates.

1) three-dimensional space vector in $\alpha\beta\gamma$ coordinates.

The large-signal average models of the four-leg voltage-source inverter are used to find the reference voltage vector for 3-D SVM in steady state, and for control shown in Fig. 4.36.

The AC terminal voltages and DC terminal and current of the four-leg switching, a switching function is defined as Equation (4.30).

$$s_{jf} = \begin{cases} 1, & if \ \left(s_{jp} \ and \ s_{fn}\right) are closed \\ 0, & if \ \left(s_{jp} \ and \ s_{fp}\right) or \ \left(s_{jn} \ and \ s_{fn}\right) are closed \\ -1, & if \ \left(s_{jn} \ and \ s_{jf}\right) and closed \end{cases} \tag{4.41}$$

where $j = \{a, b, c\}$.

Therefore, the instantaneous AC terminal voltage v_{af}, v_{bf}, v_{cf} and the DC terminal current i_p can be expressed as

$$\begin{bmatrix} v_{af} & v_{bf} & v_{cf} \end{bmatrix}^T = \begin{bmatrix} s_{af} & s_{bf} & s_{cf} \end{bmatrix}^T g V_d, \tag{4.42}$$

$$i_p = \begin{bmatrix} s_{af} & s_{bf} & s_{cf} \end{bmatrix} g \begin{bmatrix} i_a & i_b & i_c \end{bmatrix}^T, \tag{4.43}$$

where V_d is the DC link voltage.

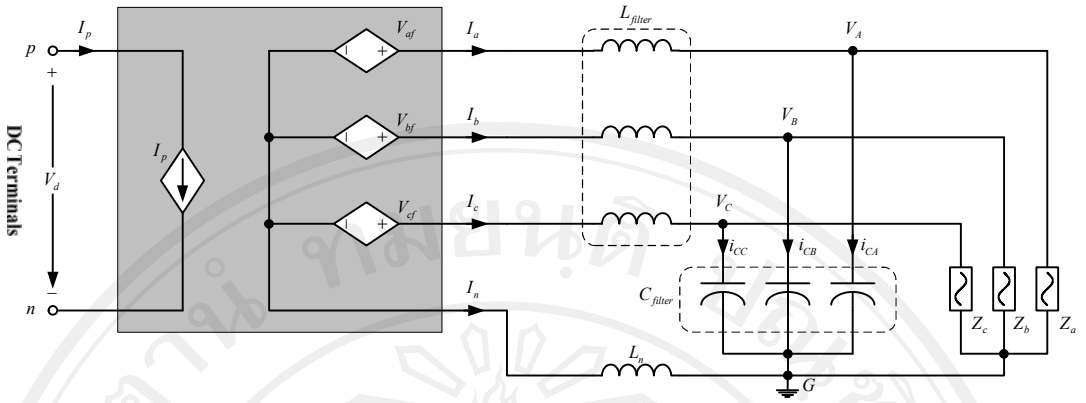

Figure 4.36 Average large-signal model of four-leg inverter.

The averaged ac terminal voltage V_{af}, V_{bf} and V_{cf} and the DC terminal current I_p are expressed as [15]

$$\begin{bmatrix} V_{af} & V_{bf} & V_{cf} \end{bmatrix}^T = \begin{bmatrix} d_{af} & d_{bf} & d_{cf} \end{bmatrix}^T V_d , \tag{4.44}$$

$$I_p = \begin{bmatrix} d_{af} & d_{bf} & d_{cf} \end{bmatrix} \cdot \begin{bmatrix} I_a & I_b & I_c \end{bmatrix}^T , \tag{4.45}$$

where d_{af}, d_{bf} and d_{cf} are line-to-neutral duty ratios.

From the large-signal average circuit model of the four-leg inverter in Fig. 4.36, we have

$$\begin{bmatrix} V_{af} \\ V_{bf} \\ V_{cf} \end{bmatrix} = \begin{bmatrix} L\left(\frac{dI_a}{dt} + C\frac{d^2V_{AG}}{dt^2}\right) + V_{AG} - L_n\frac{dI_n}{dt} \\ L\left(\frac{dI_b}{dt} + C\frac{d^2V_{BG}}{dt^2}\right) + V_{BG} - L_n\frac{dI_n}{dt} \\ L\left(\frac{dI_c}{dt} + C\frac{d^2V_{CG}}{dt^2}\right) + V_{cG} - L_n\frac{dI_n}{dt} \end{bmatrix}, \tag{4.46}$$

$$I_n = -\left(I_a + I_b + I_c\right) - C\frac{d\left(V_{AG} + V_{BG} + V_{CG}\right)}{dt}, \tag{4.47}$$

where I_a, I_b and I_c are three-phase load current,
I_n is the neutral current.

Compared to the traditional three-leg inverter which has eight switching state vectors, the four-leg inverter has sixteen switching state vectors. This switching state vectors are shown in Fig.4.37 in the space of transformed phase voltage $\{V_{af}, V_{bf}, V_{cf}\}$,

where α,β plane is the plane in which $V_{af}+V_{bf}+V_{cf}=0$, and γ is the axis of the zero sequence component.

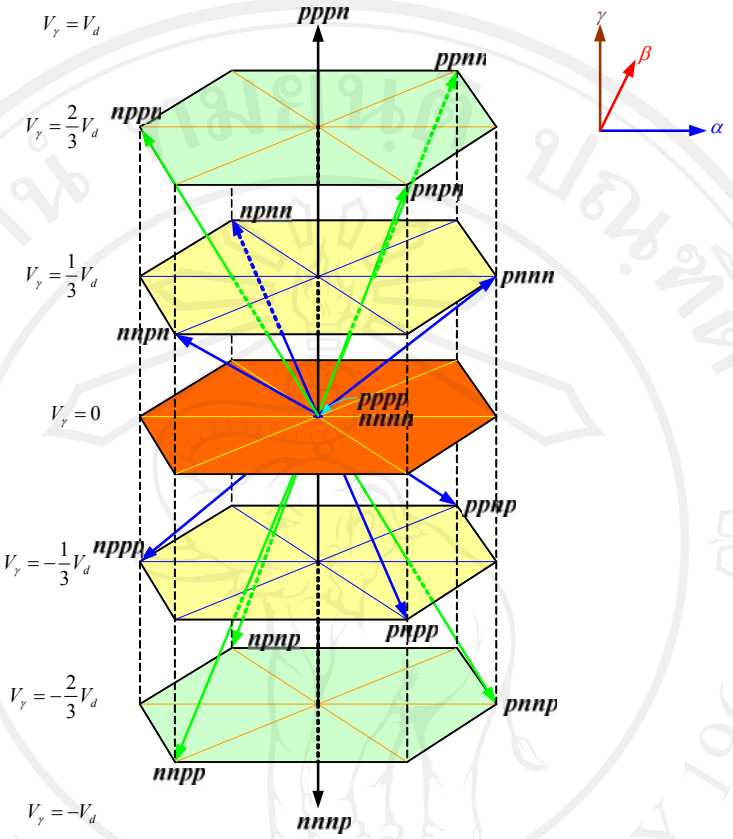

Figure. 4.37 Switching vectors of a four-leg inverter.

Each vector corresponds to a particular switching combination denoted with a four letter code (e.g. pnpp) corresponding to the four nodes (a, b, c, f) respectively, being connected either to the positive (p) or the negative (n) DC rail. The projection of these sixteen switching state vectors into the α,β plane forms the switching state hexagon as shown in Fig. 4.38.

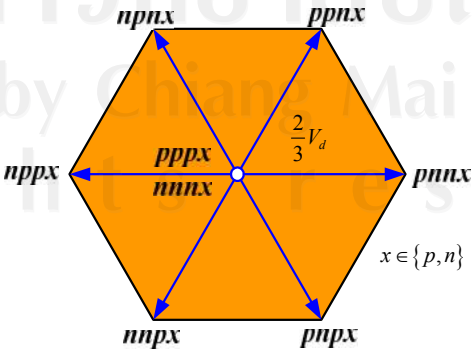

Figure. 4.38 Projection of the sixteen vectors into α,β plane.

The disadvantages of 3D space vector modulation based on $\alpha\beta\gamma$ coordinate are as follow:[11]

- The change of reference frame has to be carried out, implying complex calculations.
- The three-dimensional representation of the switching vector in $\alpha\beta\gamma$ is difficult to understand. It dose not offer a clear picture of the vector positions in the space.
- Most methods based on $\alpha\beta\gamma$ representation need to determine the sextant in which the desired voltage vector is included, which leads to many complicated operations, including rotations, complex comparisons and so forth.

2) Three-dimensional space vectors modulation in *abc* coordinates.

Most of three-dimensional space vectors use a representation of voltage vector in $\alpha\beta\gamma$ coordinate, instead of using *abc* coordinate. This representation offers interesting information about the zero sequence component of both currents and voltages (proportional to the γ coordinate), however it has some drawbacks as described in previous section.

The four-leg inverter phase-neutral voltage $\left(V_{af}, V_{bf}, V_{cf}\right)$ are decoupled, have to be expressed in a three-dimensional space. For doing the representation, one chooses these phase voltages V_{af}, V_{bf}, V_{cf} as reference frame. Then, the switching vectors present a very simple and straightforward expression as in Equation (4.48)[11], that depends on the discrete functions s_i

$$V_{abc} = \begin{bmatrix} V_a - V_f \\ V_b - V_f \\ V_c - V_f \end{bmatrix} = V_d \begin{bmatrix} s_a - s_f \\ s_b - s_f \\ s_c - s_f \end{bmatrix}. \tag{4.48}$$

These functions are directly the gating signals of the upper switch of each branch, with value $\{0,1\}$ depending on whether or not the lower or upper switch of the i leg is connected, as it is depicted in Fig.4.38.

Using this representation, it is very easy to notice that the vectors are all in the vertices of two cubes, with an edge length of one: one of them is placed in the “all positive” region of the space defined (vector 1 – 8) and other one is in the “all negative” region of the space defined (vector 9 – 16), as represented in Fig. 4.39.

Table 4.1. Switching states, voltage terminals and switching vector in *abc* coordinates.

Stage	s_f	s_a	s_b	s_c	V_{af}	V_{bf}	V_{cf}	Vector
1	0	0	0	0	0	0	0	V1
2	0	0	0	1	0	0	1	V2
3	0	0	1	0	0	1	0	V3
4	0	0	1	1	0	1	1	V4
5	0	1	0	0	1	0	0	V5
6	0	1	0	1	1	0	1	V6
7	0	1	1	0	1	1	0	V7
8	0	1	1	1	1	1	1	V8
9	1	0	0	0	-1	-1	-1	V9
10	1	0	0	1	-1	-1	0	V10
11	1	0	1	0	-1	0	-1	V11
12	1	0	1	1	-1	0	0	V12
13	1	1	0	0	0	-1	-1	V13
14	1	1	0	1	0	-1	0	V14
15	1	1	1	0	0	0	-1	V15
16	1	1	1	1	0	0	0	V16

The planes that define the control region, in which the voltage vectors will be included, present very simple expressions. Six of them are parallel to the coordinate planes, express by the equation $V_a = \pm 1, V_b = \pm 1$ and $V_c = \pm 1$. These planes express the conditions that force the line voltage to be less than or equal to the DC link voltage.

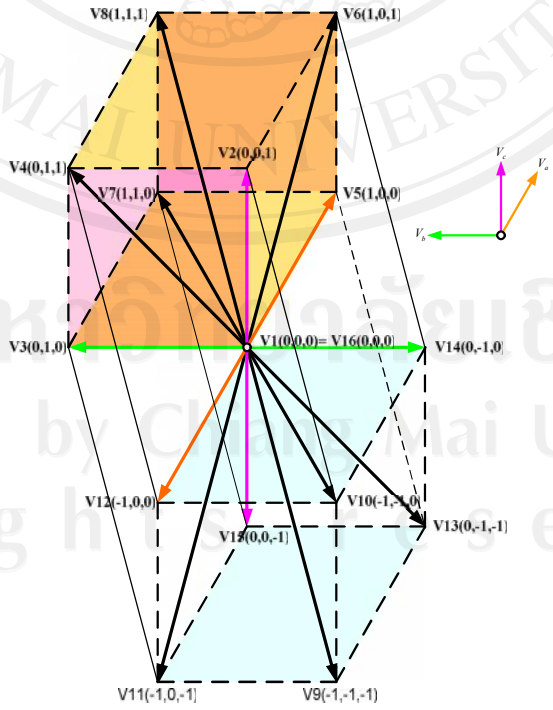

Figure 4.39 Switching vector base on *abc* coordinate.

The space vector modulation algorithm based on *abc* coordinates is used to generate the reference voltage with the sixteen switching vectors shown in Table 4.1. The dodecahedron in Fig. 4.38 can be split into 24 tetrahedrons, each of them containing three nonzero switching vectors along with the zero(double) vectors. Once the tetrahedron is chosen, appropriate switching vectors could be used to synthesize the reference vector. A very efficient way to make the selection of the tetrahedron is presented as,

$$\begin{cases} C_1 = Sign\left(INT\left(v_{a\_ref}+1\right)\right) \\ C_2 = Sign\left(INT\left(v_{b\_ref}+1\right)\right) \\ C_3 = Sign\left(INT\left(v_{c\_ref}+1\right)\right) \end{cases}$$
$$\begin{cases} C_4 = Sign\left(INT\left(v_{a\_ref}-v_{b\_ref}+1\right)\right) \\ C_5 = Sign\left(INT\left(v_{b\_ref}-v_{c\_ref}+1\right)\right) \\ C_6 = Sign\left(INT\left(v_{a\_ref}-v_{c\_ref}+1\right)\right) \end{cases} \quad (4.49)$$

where

$INT(x)$	is the integer part of x
$Sign(x)$	extracts the sign of x, being 1 if x positive, -1 if negative and 0 if $x=0$
$v_{a\_ref}, v_{b\_ref}, v_{c\_ref}$	is the reference voltage vector, normalized with V_d.

The pointer to the region in which the reference vector is included can be calculated as

$$RP = 1 + \sum_{i=1}^{6} C_i \times 2^{(i-1)} \quad (4.50)$$

The *RP*, from Equation (4.51) ranges 1 – 64 , will adopt only one of 24 different possible values that correspond to the 24 tetrahedrons, each of them is composed of three nonzero switching vectors(NZSV) $(Vd1, Vd2, Vd3)$ and the double zero voltage vector $(Vd0)$ as shown in Table 4.2 [12].

Table 4.2 The duty cycle calculation, Region Pointer, non-zero switching vectors.

RP	*Vd1*	*Vd2*	*Vd3*	*d1*	*d2*	*d3*
1	V9	V10	V12	$-V_{c\_ref}$	$-V_{b\_ref}+V_{c\_ref}$	$-V_{a\_ref}+V_{b\_ref}$
5	V2	V10	V12	V_{c_ref}	$-V_{b\_ref}$	$-V_{a\_ref}+V_{b\_ref}$
7	V2	V4	V12	$-V_{b\_ref}+V_{c\_ref}$	V_{b_ref}	$-V_{a\_ref}$
8	V2	V4	V8	$-V_{b\_ref}+V_{c\_ref}$	$-V_{a\_ref}+V_{b\_ref}$	V_{a_ref}
9	V9	V10	V14	$-V_{c\_ref}$	$-V_{a\_ref}+V_{c\_ref}$	$V_{a\_ref}-V_{b\_ref}$
13	V2	V10	V14	V_{c_ref}	$-V_{a\_ref}$	$V_{a\_ref}-V_{b\_ref}$
14	V2	V6	V14	$-V_{a\_ref}+V_{c\_ref}$	V_{a_ref}	$-V_{b\_ref}$
16	V2	V6	V8	$-V_{a\_ref}+V_{c\_ref}$	$V_{a\_ref}-V_{b\_ref}$	V_{b_ref}
17	V9	V11	V12	$-V_{b\_ref}$	$V_{b\_ref}-V_{c\_ref}$	$-V_{a\_ref}+V_{c\_ref}$
19	V3	V11	V12	V_{b_ref}	$-V_{c\_ref}$	$-V_{a\_ref}+V_{c\_ref}$
23	V3	V4	V12	$V_{b\_ref}-V_{c\_ref}$	V_{c_ref}	$-V_{a\_ref}$
24	V3	V4	V8	$V_{b\_ref}-V_{c\_ref}$	$-V_{a\_ref}+V_{c\_ref}$	V_{a_ref}
41	V9	V13	V14	$-V_{a\_ref}$	$V_{a\_ref}-V_{c\_ref}$	$-V_{b\_ref}+V_{c\_ref}$
42	V5	V13	V14	V_{a_ref}	$-V_{c\_ref}$	$-V_{b\_ref}+V_{c\_ref}$
46	V5	V6	V14	$V_{a\_ref}-V_{c\_ref}$	V_{c_ref}	$-V_{b\_ref}$
48	V5	V6	V8	$V_{a\_ref}-V_{c\_ref}$	$-V_{b\_ref}+V_{c\_ref}$	V_{b_ref}
49	V9	V11	V15	$-V_{b\_ref}$	$-V_{a\_ref}+V_{b\_ref}$	$V_{a\_ref}-V_{c\_ref}$
51	V3	V11	V15	V_{b_ref}	$-V_{a\_ref}$	$V_{a\_ref}-V_{c\_ref}$
52	V3	V7	V15	$-V_{a\_ref}+V_{b\_ref}$	V_{a_ref}	$-V_{c\_ref}$
56	V3	V7	V8	$-V_{a\_ref}+V_{b\_ref}$	$V_{a\_ref}-V_{c\_ref}$	V_{c_ref}
57	V9	V13	V15	$-V_{a\_ref}$	$V_{a\_ref}-V_{b\_ref}$	$V_{b\_ref}-V_{c\_ref}$
58	V5	V13	V15	V_{a_ref}	$-V_{b\_ref}$	$V_{b\_ref}-V_{c\_ref}$
60	V5	V7	V15	$V_{a\_ref}-V_{b\_ref}$	V_{b_ref}	$-V_{c\_ref}$
64	V5	V7	V8	$V_{a\_ref}-V_{b\_ref}$	$V_{b\_ref}-V_{c\_ref}$	V_{c_ref}

The calculation of the duty cycle can be express as:

$$d = M_d^{-1} V_{ref} \tag{4.51}$$

where $V_{ref} = \begin{bmatrix} V_{af} \\ V_{bf} \\ V_{cf} \end{bmatrix}$, $d = \begin{bmatrix} d1 \\ d2 \\ d3 \end{bmatrix}$,

$$M_d = \begin{bmatrix} Vd1_a, Vd2_a, Vd3_a \\ Vd1_b, Vd2_b, Vd3_b \\ Vd1_c, Vd2_c, Vd3_c \end{bmatrix}.$$

The duty cycles of the zero vector $d4 = 1 - d1 - d2 - d3$. Based on a minimum harmonic criterion, the switching vectors are distributed symmetrically along the middle of the switching period.

The duty cycle calculations imply only addition or subtraction of reference vector components, as in Table 4.2. Once the *RP* is obtained, the switching vector and the duty cycles could be calculated directly, according to the reference voltage.

The calculation of *RP* according to the space vector modulation theory by judging the positive and negative relationship among the three phase reference voltage V_{af}, V_{bf}, V_{cf} we could know:

1. if $V_{af} > 0$, then $C_1 = 1$, Else $C_1 = 0$
2. if $V_{bf} > 0$, then $C_2 = 1$, Else $C_2 = 0$
3. if $V_{cf} > 0$, then $C_3 = 1$, Else $C_3 = 0$
4. if $V_{ab} > 0$, then $C_4 = 1$, Else $C_4 = 0$
5. if $V_{bc} > 0$, then $C_5 = 1$, Else $C_5 = 0$
6. if $V_{ac} > 0$, then $C_6 = 1$, Else $C_6 = 0$

The calculating of region pointer (*RP*) is shown in Fig.40 and *RP* compare with voltage phase A(positive magnitude is 20%) shown in Fig. 4.41.

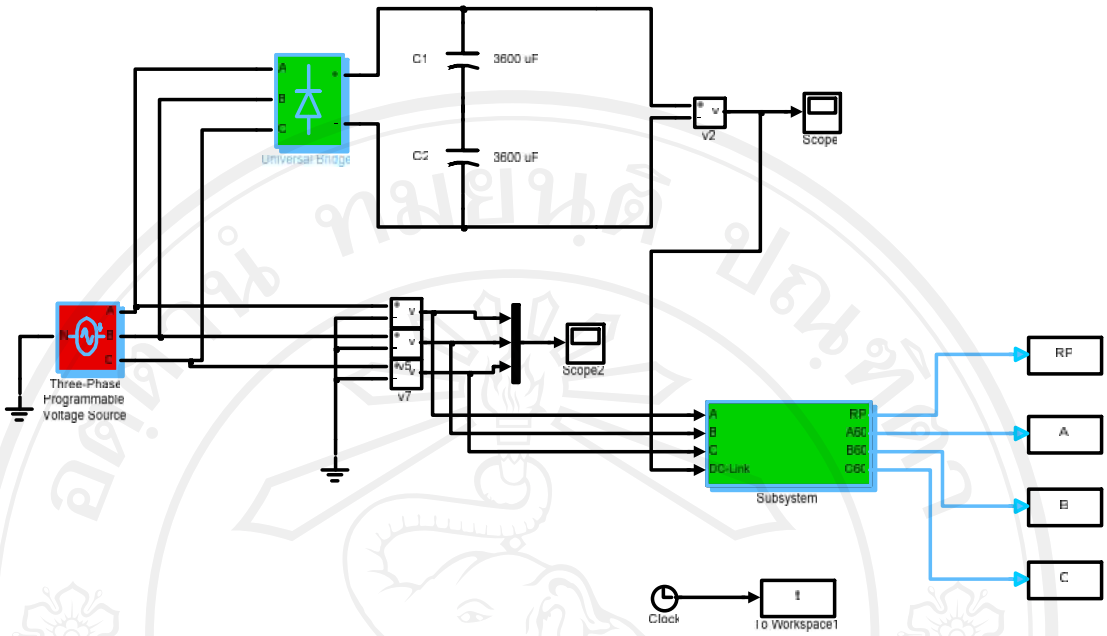

Figure. 4.40 The simulation model of region pointer(*RP*) calculate.

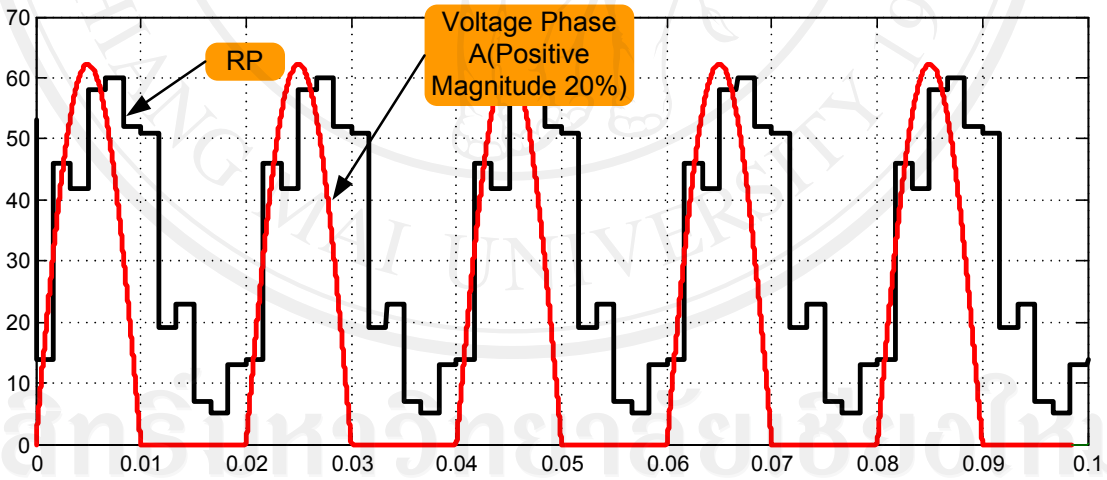

Figure 4.41 The region pointer compare with phase A voltage (positive magnitude 20%)

The region pointer sequence start from 14, 46, 42, 58, 60, 52, 51, 19, 23, 7, 5, 13 and 14, 46 then repeated. The results of experiments are shown in Fig. 4.42 and the sequence of *RP* is shown in Fig 4.43.

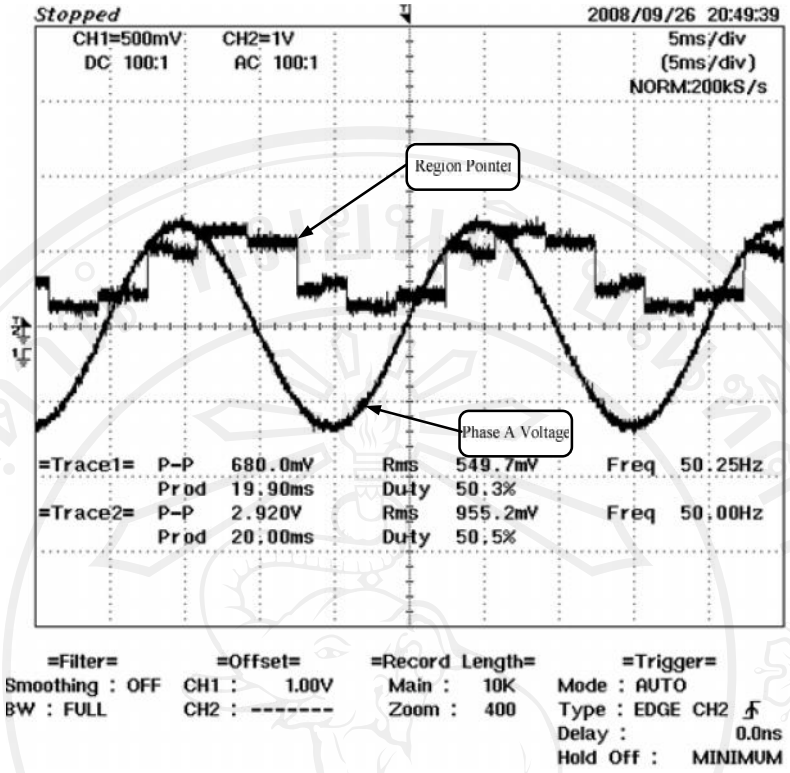

Figure 4.42 The region pointer form dsPIC30F6010 and phase A voltage.

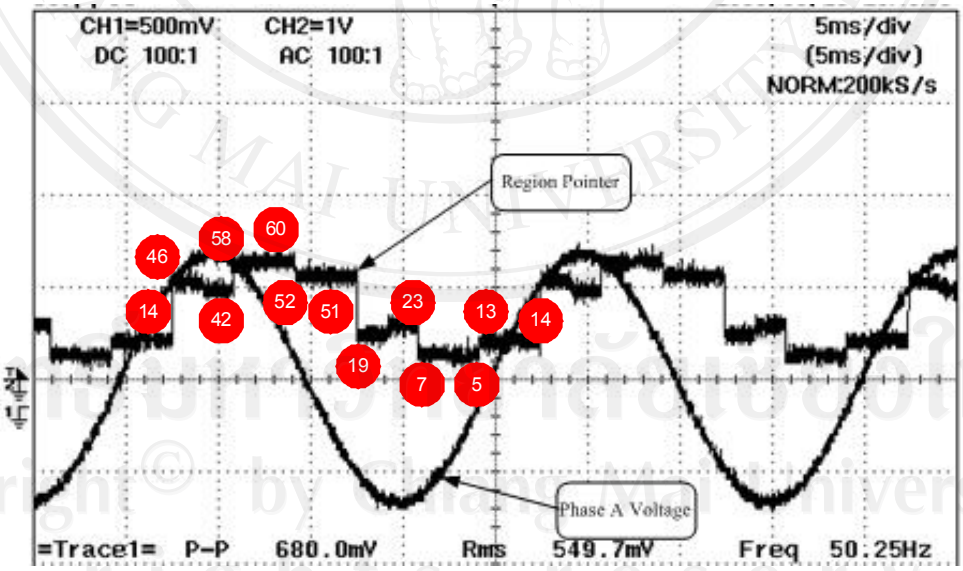

Figure 4.43 The sequence of region pointer (*RP*).

The calculation of *RP* also requires very low computation effort, as it can be done by merely comparing and adding number. Implementing these equations on a common microprocessor dsPIC30F6010 @50 MHz, it takes only 20 operations (that

is $0.8\,\mu s$) to select the correct therahedron. To make the same operation in $\alpha\beta\gamma$ coordinates[2], a minimum of $4\mu s$ is needed.

Having obtain the duty cycles of the switching vectors, the duty cycles of each upper switching $\left(s_{ap}, s_{bp}, s_{cp}, s_{fp}\right)$ could be easily calculated.

For example the RP = 46, then the reference vector would be composed of three nonzero vectors V5, V6, V14 and two zero vectors, V1, V16 as shown in Fig.4.44.

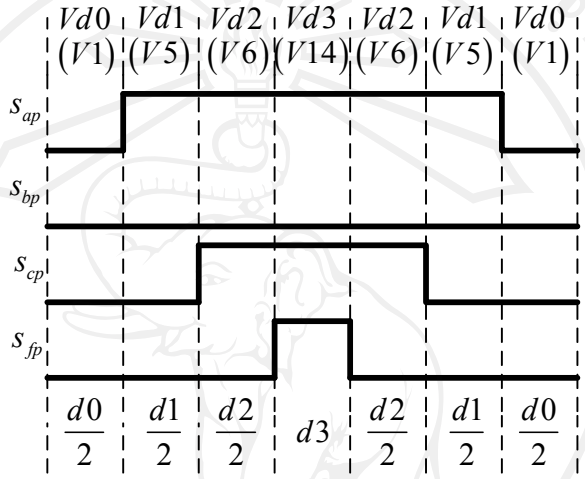

Figure 4.44 Switching signals to produce a voltage vector in region $RP = 46$.

Using Equation (4.40) the duty cycles $d1, d2, d3$ and $d0$ cad be computed and they are shown in Fig. 4.45.

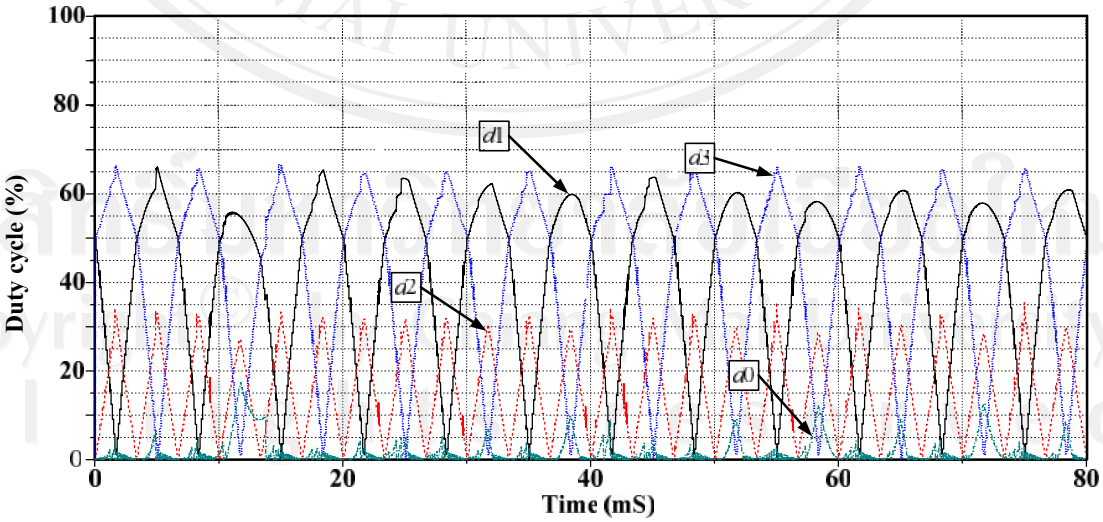

Figure 4.45 The duty cycles $d1, d2, d3$ and $d0$ from simulation program.

This thesis used a 3D space vector modulation algorithm in the *abc* coordinates. The algorithm avoids complex coordinates conversion makes the calculation of the duty cycle much easier.

The *abc* algorithm to get the reference voltage are described in detail. The given reference voltages are calculated timely by the load currents and bus voltage, so the inverter could work on variable load conditions.

4.2.4.3 Design of 3-phase 4-wire 4-leg inverter

Specification

The design targets of the 3-phase 4-wire 4-leg inverter are as follows:

- Output Voltage : 220 V/380 V
- Output frequency: 50 Hz
- Output power : 3 kVA(three phase)
- Maximum per-phase power: 1 kVA
- Switching frequency: 3 kHz
- Load unbalance: negative-sequence unbalance $\leq 100\%$
  zero-sequence unbalance $\leq 33\%$

1) DC Link Voltage

In a practical design, the selection of the DC link voltage V_d is a trade-off between power switch voltage stress and control headroom for transients. The negative sequence reference voltage, hence, the negative-sequence load current, imposes a significant impact on the selection of the DC link voltage. Considering a 10% control overhead for transient, DC link for 220 V line-to-neutral output AC voltage, resulted DC link voltage would be $220 \times \sqrt{2} \times \sqrt{3} = 592\,\text{V}$. It seems that a $600\,\text{V}$ DC bus would be enough.

2) DC Link Capacitor

Since the zero-sequence load current will be handled by the fourth neutral leg, only the negative-sequence load current is reflected to the DC link capacitor. Design of the DC link capacitance can use Equation (4.41). Considering 100% negative-sequence unbalance, and 7 V of the maximum allowed voltage ripple -1.1% of the rated DC link voltage, the resulting DC link capacitor is $470\mu F$.

$$C_{DC\_Link} = \frac{\sqrt{3} m I_o}{4 \omega_{ripp} \Delta V_g} \tag{4.52}$$

m is modulation index
I_o is negative-sequence current
ω_{ripp} is ripple frequency (2ω)

where: $I_o = 3000 / \sqrt{2} \times 220 = 7.87\,\text{A}$ (100% negative-sequence current)
$m = 0.6$, $\Delta V_g = 7\,\text{V}$

$$\omega_{ripp} = 2\omega = 2 \times 2 \times \pi \times 50 = 628\,\text{rad/s}$$

$$\therefore \qquad C_{DC\_Link} = \frac{\sqrt{3} \times 0.6 \times 7.87}{4 \times 628 \times 7} = 465\,\mu\text{F}$$

Selected: $C_{DC\_Link} = 470\,\mu\text{F}$

3) Switching frequency

Switching frequency needs to be selected as high as possible from a control point of view, as long as there is no thermal issue. In order to find the optimum switching frequency, switching losses of power devices need to be evaluated. Based on the estimated conduction loss and the switching losses, a 3 kHz switching frequency is selected.

4) Power Switch

In this thesis we used the power MOSFET IPFP460PbF, $V_{DSS} = 500\,\text{V}$, $I_D = 20\,\text{A}$.

5) AC Output Lowpass Filter

L and C form a 2nd –order filter with -40dB/dec attenuation to the switching ripples. With the 3 kHz switching frequency, the resonance frequency f_{res} is selected as 300 Hz to have less than 15% of voltage ripple at switching frequency. In this thesis $L_f = 4\,\text{mH}$ and $C_f = 470\,\mu\text{F}$ was used. The resonance frequency f_{res} is:

$$f_{res} = \frac{1}{2\pi\sqrt{L_f C_f}}$$

$$f_{res} = \frac{1}{2\pi\sqrt{4 \times 10^{-3} \times 470 \times 10^{-6}}} = 116.08\,\text{Hz}$$

The resonance frequency is less than 1% of switching frequency.

6) 3-phase 4-wire 4-leg inverter controller

The 3-phase 4-wire 4-leg inverter is controlled by a dsPIC30F6010 microcontroller. The circuit diagram of dSPIC30F6010 microcontroller is shown in Fig.4.46. The hardware of 3-phase 4-wire 4-leg inverter and dSPIC30F6010 microcontroller was shown in Fig. 4.47. The LC low-pass filter of 3-phase 4-wire 4-leg inverter was shown in Fig. 4.48.

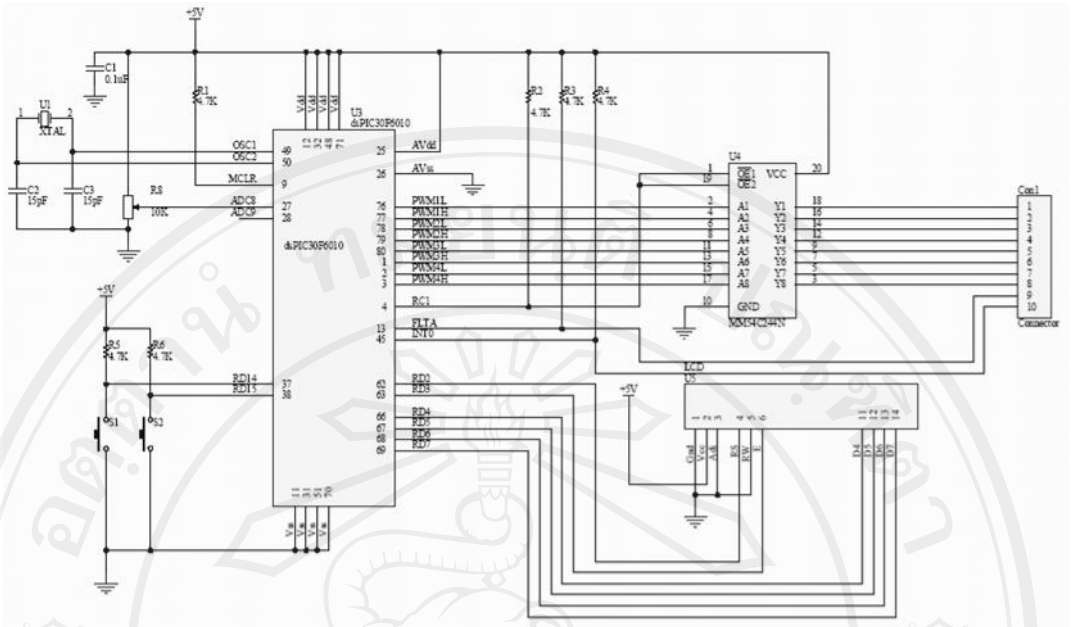

Figure 4.46 The circuit diagram of dsPIC30F6010 microcontroller.

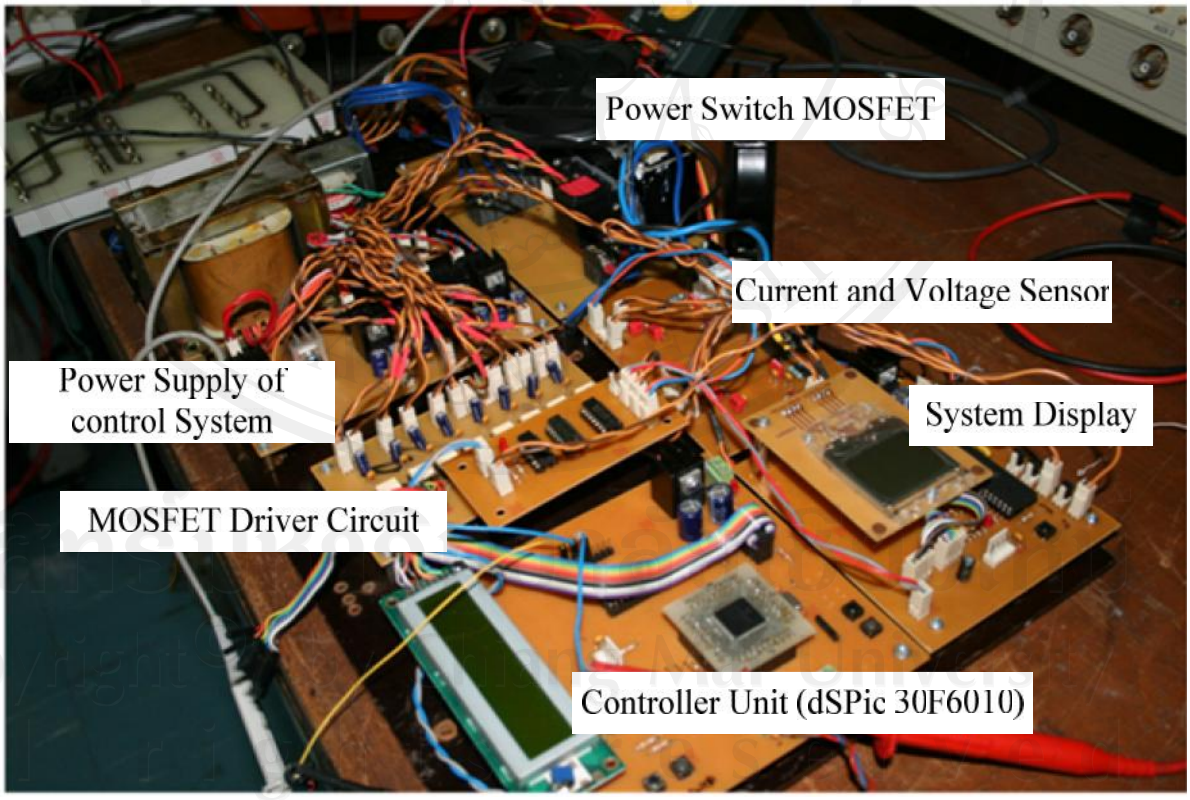

Figure 4.47 The 3-phase 4-wire 4-leg inverter and dsPIC30F6010 microcontroller.

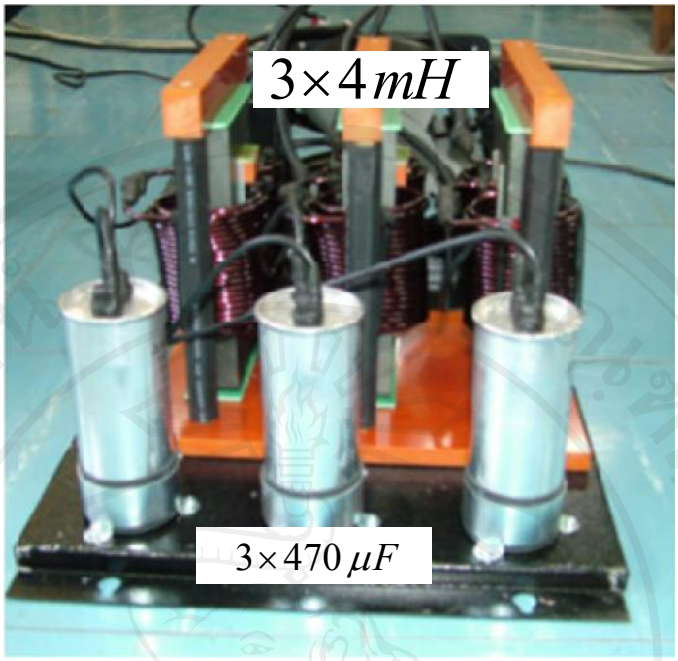

Figure 4.48 The LC low-pass filter of 3-phase 4-wire 4-leg inverter.

4.3 Conclusion

This thesis has constructed 3-phase 4-wire voltage sag compensation based on three-dimensional space vector modulation technique on *abc* coordinates. The operations of voltage sag compensation are verified through the 3-phase 4-wire 4-leg inverter controlled with three-dimensional space vector modulation in *abc* coordinate to regulate the neutral current. Depending upon the voltage sag situation, a boost chopper converts the unregulated DC to a regulated DC link voltage. The constant DC link voltage is converted by 3-phase 4-wire 4-leg inverter to a maintained AC voltage. The proposed 3-phase 4-wire voltage sag compensation has been implemented and experiment results are shown in next chapter.