CHAPTER 5
Proposed Voltage Sag Compensator Using Back-to-Back Converters

5.1 Introduction

Nowadays, several ideas have been reported for compensation of voltage disturbances and the majority of solutions are concerned with voltage sags. Some approaches use dynamic voltage restorer by means of energy storage devices and power transformers [2], [9]. Some use boost or buck-boost converters incorporating with inverter [3], [41], which introduced the input current distortion during voltage sags. Some concepts use interphase AC-AC topology by means of AC choppers and isolation power transformers [10]. However, the point of common coupling (PCC) may experience noise due to ac chopper circuit. Some methods use AC/AC PWM converter incorporating with an autotransformer [11], the power transformer is still required in these methods.

In [2], [3], [9]-[11], [41], among the conventional voltage sags compensation, the boost converter based compensator has distinguished advances such as long duration and deep sag compensation, special energy storages and power transformers are eliminated.

A conventional boost converter based compensator consists of a three-phase full-bridge rectifier, a boost converter, a three-phase PWM inverter, and two bypass circuits [3]. The rectifier and the boost convert the input voltage sag into the DC-link voltage with PWM strategy. On the other hand, the inverter converts the dc-link voltage into the output voltage with PWM strategy. Therefore, the regulated sinusoidal output voltage can be achieved. The set of AC/DC/AC converters is operated when sag of the input voltage occurs. However, the drawback of this circuit topology is caused by the boost converter. In practice, it is difficult to design a boost converter with high step-up gain due to the equivalent series resistance (ESR) element that causes poor efficiency and degraded voltage gain. Other drawback is the obtaining of the low power factor and high harmonic distortion of the utility supply currents due to the conventional three-phase full-bridge rectifier operation. A poor power quality is then made during voltage sag compensation.

In this thesis, the proposed voltage sag compensator is presented. In the proposed voltage sag compensator, long duration and deep sag compensation are available and special energy storages and power transformers are eliminated. High power factor and low harmonic distortion of input current is obtained [41].

5.2 Principles of Operation

The proposed voltage sag compensator is shown in Figure 5.1. It consists of two STS, i.e. the main static transfer switch and the auxiliary static transfer switch, back-to-back converters as supply-side converter (PWM rectifier) and load-side converter (Inverter), and *LC* filter.

In the normal incident, grid voltages directly feed the power to load via the main STS. Whenever the voltage sags occur, the main STS is opened (turned off) to disconnect load from grid voltages and then the auxiliary STS is closed (turned on) to the inverter and load. It can be noted that in this incident, load is fed the power from the inverter instead of the faulted grid voltages during voltage sag occurrences. The power feed to the load with no interruption and continuous operation is available.

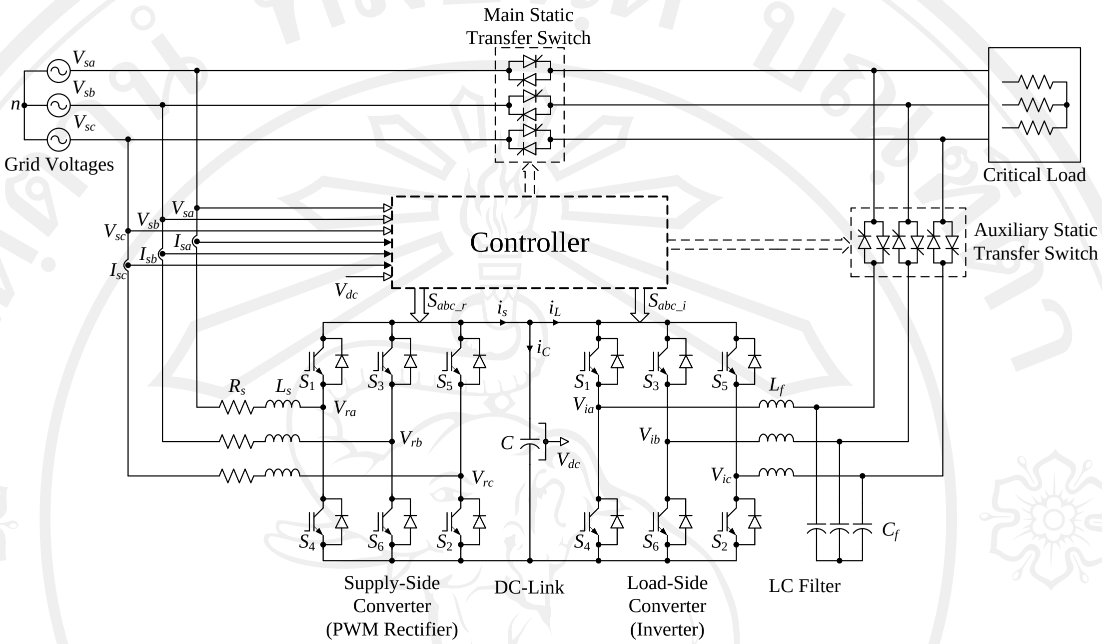


Figure 5.1 Configuration of the proposed voltage sag compensator using back-to-back converters.

Whenever the voltage sag is cleared, the reverse operation is taken place by turning off the auxiliary STS and turning on the main STS, the load is then fed from the healthy grid voltages again.

The transition from grid voltages to PWM rectifier and inverters is seamless by means of STS. The three-phase output voltage of the inverter is synchronized with the grid voltages.

In this proposed voltage compensator, while the PWM rectifier performs a voltage rectification from the AC grid voltages to a constant DC-link voltage, the inverter is performing a voltage inversion from the constant DC-link voltage to AC load voltages. It can be considered that PWM rectifier is a major part of the proposed voltage sag compensator since DC-link voltage must be kept constant regardless of varying grid voltages. To accomplish this goal, the vector control scheme is applied to the PWM rectifier for the reasons of fast and accuracy of the DC-link voltage control, low total harmonic distortion and high power factor of the input currents. A small input filter (L_s) can be designed to absorb the high frequency harmonics injected into the grid voltages by the rectifier switching action. Due to constant DC-link voltage the open loop scheme can be applied to the inverter.

This voltage sag compensator advantages are not using of special energy storage devices or transformers which is different from several methods [2], [9]-[11], ability to compensate deep and long-duration voltage sags, the grid currents have low total harmonic distortion and the input power factor is maintained to be nearly unity.

5.3 Control Method

5.3.1 Control strategy of PWM rectifier

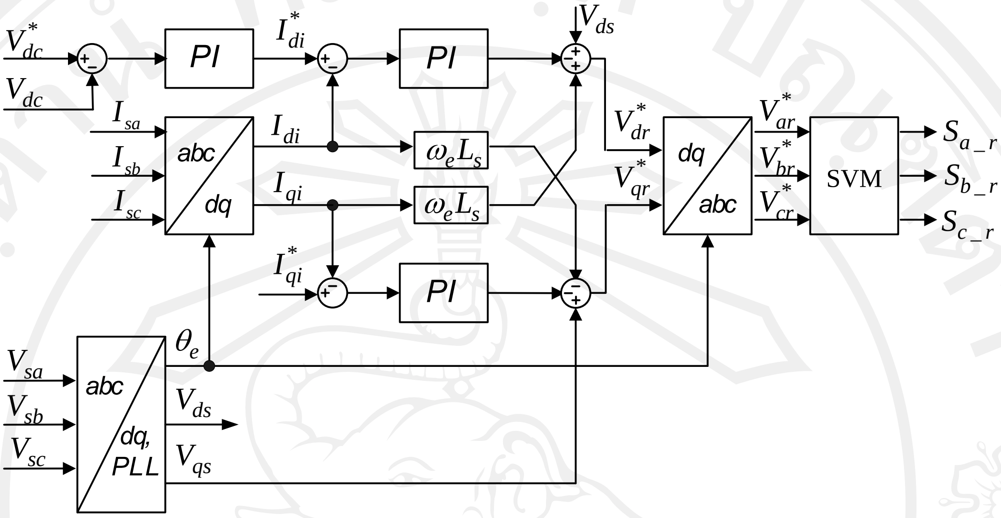


Figure 5.2 Control strategy of PWM rectifier.

As shown in Figure 5.2, the control scheme of PWM rectifier contains internal current regulation loops and external DC-link voltage control loop. The objective of PWM rectifier is to keep the DC-link voltage constant regardless of the variation of grid voltages. To achieve this purpose, a vector control is adopted. The supply voltages can be expressed as follows:

$$\begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} = R_s \begin{bmatrix} I_{sa} \\ I_{sb} \\ I_{sc} \end{bmatrix} + L_s \frac{d}{dt} \begin{bmatrix} I_{sa} \\ I_{sb} \\ I_{sc} \end{bmatrix} + \begin{bmatrix} V_{ra} \\ V_{rb} \\ V_{rc} \end{bmatrix} \tag{5.1}$$

where V_{sa}, V_{sb}, V_{sc} are the grid phase voltages, V_{ra}, V_{rb}, V_{rc} are the converter phase voltages, I_{sa}, I_{sb}, I_{sc} are grid phase currents, R_s and L_s are the grid voltage resistor and inductor, respectively. Having the *abc-dq* transformation [18], the grid voltages in the *dq* reference frame equations are obtained.

$$\begin{bmatrix} V_{ds} \\ V_{qs} \end{bmatrix} = R_s \begin{bmatrix} I_{di} \\ I_{qi} \end{bmatrix} + L_s \frac{d}{dt} \begin{bmatrix} I_{di} \\ I_{qi} \end{bmatrix} + \begin{bmatrix} 0 & -w_e L_s \\ w_e L_s & 0 \end{bmatrix} \begin{bmatrix} I_{di} \\ I_{qi} \end{bmatrix} + \begin{bmatrix} V_{dr} \\ V_{qr} \end{bmatrix} \tag{5.2}$$

where V_{ds}, V_{qs} are the $d-q$ axis grid voltages, V_{dr}, V_{qr} are the $d-q$ axis converter voltages, I_{ds}, I_{qs} are the $d-q$ axis grid currents. From (5.2), it can be seen that the $d-q$ axis voltages are cross coupled by terms $-w_e L_s I_{qi}$ and $w_e L_s I_{di}$, respectively.

The grid voltage angle has to be determined. By definition, the grid voltage angle is as follows:

$$\theta_e = \int \omega_e dt = \tan^{-1}\frac{V_\beta}{V_\alpha}, \tag{5.3}$$

where V_α, V_β are the $\alpha - \beta$ axis grid voltages, ω_e is the grid voltage angular frequency, $\omega_e = 2\pi f_e$, and θ_e is the grid voltage vector position. The angular position can be also achieved from by the Phase Locked Loop (PLL).

The DC power has to be equal to the active power flowing between the grid voltages and the DC-link inverter. Thus, it can be presented as follows:

$$V_{dc} I_s = \frac{3}{2} V_{ds} I_{di}, \tag{5.4}$$

$$C\frac{dV_{dc}}{dt} = I_s - I_L, \tag{5.5}$$

where V_{dc} is the DC-link voltage, I_s is the current between the DC-link and the grid voltages, I_L is the current between the DC-link and the critical load, and C is the DC-link capacitor.

5.3.2 Control strategy of inverter

For the simple structure, the open loop scheme is applied to the inverter as shown in Figure 5.3. While V_{di} is a load voltage command, V_{qi} is set to zero and the angular position is obtained from PWM rectifier control scheme. It can be seen that if DC-link voltage is constant value, then the constant AC load voltage can be also achieved.

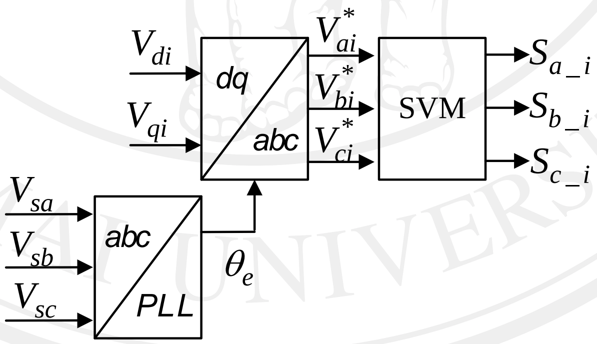


Figure 5.3 Control strategy of the inverter.

5.3.3 Voltage sag detection method

The proposed voltage sag detection method (IMSRRF-based voltage sag detection) in Chapter 3 has been used in the proposed voltage sag compensator. This voltage sag detection method is based on synchronously rotating reference frame (SRRF). The advantages of proposed voltage sag detection were fast detection, it is able to use in distorted grid voltages, and use existing data in control scheme. Figure 5.4 shows the proposed voltage detection. The sag signal was inverted the level and used to control the main static switch while the sag signal was used to directly control the auxiliary static transfer switch.

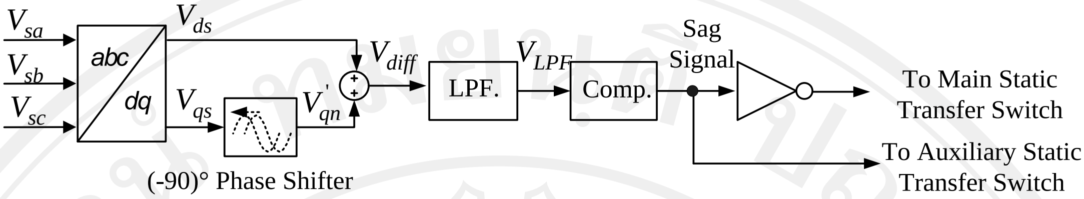


Figure 5.4 IMSRRF-based voltage sag detection.

5.4 Design criteria

In this section, the parameters and passive components used in the proposed voltage sag compensator are designed. The parameters are DC-link voltage, and PI controller gains. The passive components are PWM rectifier input inductor (L_s), inverter output filter (L_f, C_f), and DC-link capacitor (C).

5.4.1 PWM rectifier input inductor (L_s)

The high value of the input inductor of PWM rectifier will give a low current ripple but operation range of PWM rectifier is reduced. The low value of input inductor will give a high current ripple and the design is more depending on the line impedance [43].

In this thesis, the input inductor is designed as follows:

$$L_s = \frac{V_{LL}}{6\sqrt{2} f_s i_{ripple}} = 13\text{mH}, \qquad (5.6)$$

where V_{LL} is line to line rms grid voltages, f_s is switching frequency in Hz, i_{ripple} is the ripple current of the peak input current($I_{s,peak}$). $I_{s,peak}$ can be calculated from the input power and the input voltage of the back-to-back converter (1kW and 380V respectively) and i_{ripple} is selected at 20% of $I_{s,peak}$.

5.4.2 Inverter output filter (L_f, C_f)

The objective of the inverter output filter is to filter the high frequency component (i.e. switching frequency of inverter) to achieve the sinusoidal wave voltages. In this research the capacitor is selected at 10 mF and the cut-off frequency ($f_{c,LPF}$) is selected at 1kHz then the inductor can be calculated as

$$L_f = \frac{1}{(2p f_{c,LPF})^2 C_f} \quad 2.3\text{mH}, \qquad (5.7)$$

where L_f, C_f are inductor and capacitor of LC filter respectively.

5.4.3 DC-link voltage (Vdc)

The DC-link voltage is generally determined from the peak value of line-to-line grid voltages. To ensure the boost operation of PWM rectifier, the DC-link voltage must be greater than the peak value of line-to-line grid voltages. The minimum of DC-link voltage ($V_{dc,\min}$) can be calculated as follows [43]:

$$V_{dc,\min} = \sqrt{2}V_{LL}. \tag{5.8}$$

In this paper, the DC-link voltage is chosen about 30% above the $V_{dc,\min}$ [44] then the DC-link voltage is chosen as $V_{dc} = 700V$.

5.4.4 DC-link capacitor (C)

For selected value of capacitor peak ripple voltage and switching frequency then the minimum capacitor can be found as [43]:

$$C_{\min} = P_C \frac{\sqrt{2} + \sqrt{3}\dfrac{V_{LL}}{V_{dc}}}{2\sqrt{3}V_{LL}\,\mathrm{D}V_{dc}f_s} = 341\,mF\ , \tag{5.9}$$

where P_C is input power of back-to-back converter and $\mathrm{D}V_{dc}$ is DC-link ripple voltage (0.1% of DC-link ripple voltage is selected).

In this thesis the DC-link capacitor is selected at 4 times of $C_{\min}$ $(1{,}364\,mF)$.

5.4.5 PI controller gains

The DC-link voltage is controlled by using vector control scheme as shown in Figure 5.2. It can be seen that three PI controllers are used in this vector control scheme, one for DC-link voltage loop (outer loop) and two for current control loops (inner loop). In this thesis, the PI controller gains are designed by a standard method [45], [46].

The gains of PI controllers can be calculated as follows:

$$K_{pi} = \frac{L_s}{3T_s} = 43, \tag{5.10}$$

$$K_{ii} = \frac{R_s}{3T_s} = 500, \tag{5.11}$$

$$K_{pv} = \frac{C}{5T_s} = 2.72,, \tag{5.12}$$

$$K_{iv} = \frac{K_{pv}}{20T_s} = 1360, \tag{5.13}$$

where

K_{pi} and K_{ii} are proportional gain and integral gain of current loop (inner loop) respectively,

K_{pv} and K_{iv} are proportional gain and integral gain of DC-link voltage loop (outer loop) respectively,

T_s is controller sampling time,

R_s is series resistance of L_s which is 0.15 W in practice.

5.5 Simulation and Experimental Results

To confirm the operation of proposed voltage sag compensator, the model of system in Figure 5.5 was built and simulated in Matlab/Simulink computer software. The simulation model was developed based on voltage sag compensation under voltage sag with numerous types of loads.

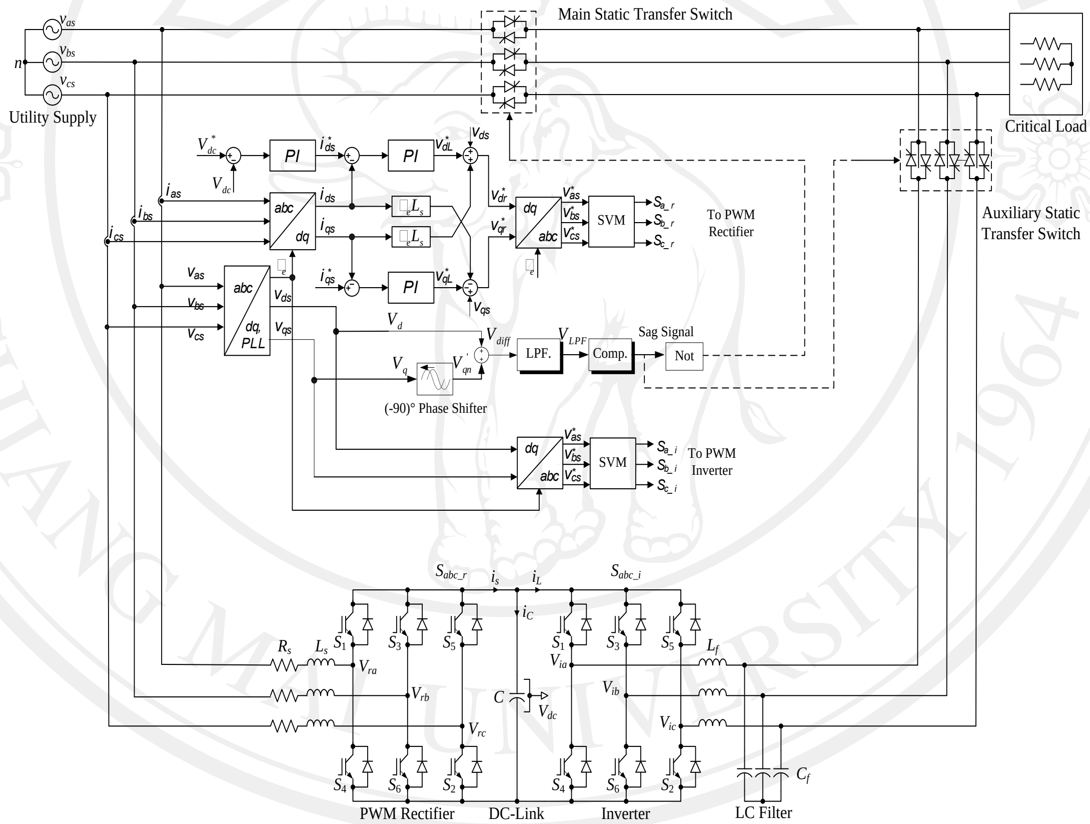


Figure 5.5 Model of the proposed voltage sag compensator for simulation.

5.5.1 Simulation and experimentation setup

Both of simulation and experimentation are set up to test the operation of voltage sag compensator that consists of PWM rectifier, inverter, voltage sag detector, and static transfer switches. The setup is shown in Figure 5.6. The voltage sag operations conditions are made. The simulation and experimental conditions are numerous types of loads.

The system parameters for the proposed voltage sag compensation system are given in Table 5.1.

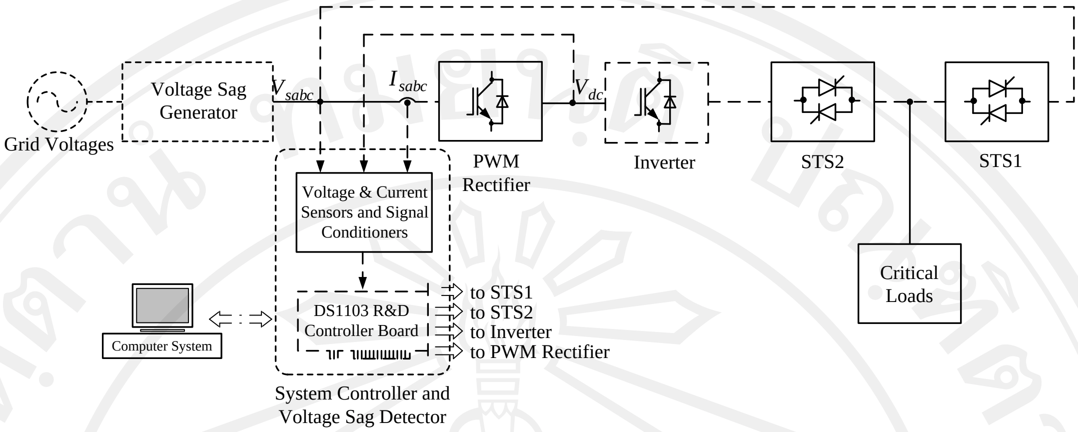


Figure 5.6 Experimental setup for proposed voltage sag compensator system test.

Table 5.1 Parameters of Voltage Sag Detection System.

Grid phase voltages, V_{sabc}	220 Vrms, 50 Hz
Voltage sag	0.7-pu three-phase sag
Cut-off frequency of low pass filters, f_c	150 Hz
PWM rectifier and inverter switching frequency, f_s	7.5 kHz
DC-link voltage (Vdc)	700 V
PWM rectifier input inductor (L_s, R_s)	13mH, 0.15W
Inverter output filter (L_f, C_f)	2.3mH, 10mF
DC-link capacitor (C)	1,360 mF
Loads	- Three-phase diode rectifier = 290 W (1.5kW) - Three-phase star inductive load = 115 W(3kW), 0.4H (3kVar)
Controller	dSPACE DS1103
Simulation/controller sampling time	100uS
Comparator hysteresis band	- Lower limit = 0.95 - Upper limit = 1.00
PI controllers Inner loop (Current) Outer loop (DC-link voltage)	 Kp = 43, Ki = 500 Kp = 2.72, Ki = 1,360
Turn-off time of STS model	100ms
STS dead time	300ms

5.5.2 Simulation results

The simulation results are shown in this section. The simulations consist of back-to-back converter operation and load compensation during three-phase voltage sag. Load types in this experimentation are three-phase rectifier load and inductive load to show the performance of the proposed voltage sag compensation system.

5.5.2.1 Back-to-back converter operation

In this section, the operation of back-to-back converter was simulated. To test the load regulation of back-to-back converter under voltage sag then static transfer switch was not included in this simulation. The measurements are determined at the input side and output side of back-to-back converter as shown in Figure 5.7. The measured parameters of input side consist of DC-link voltage (V_{dc}), converter phase input voltage (V_{sa}), and converter input current (I_{sa}).The measured parameters of input side consist of load voltage (V_o), converter phase input voltage (V_{sa}), and converter output current (I_{oa}), respectively.

In this simulation, the operations of back-to-back are shown in the period of 600 ms or 30 cycles and the extended view of waveforms (3 cycles) around grid voltage deviation period are plotted to show the detail of waveforms.

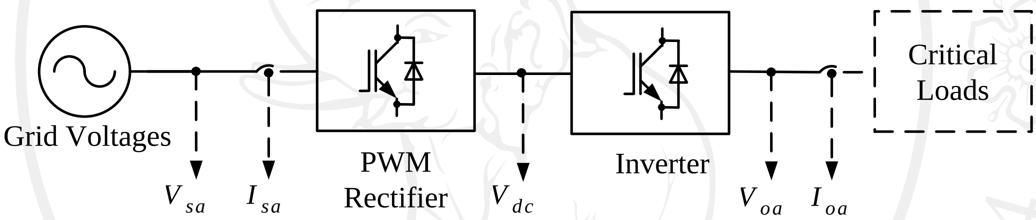


Figure 5.7 Simulation setup for back-to-back converter operation.

Figure 5.8 shows the waveforms of back-to-back converter at input side under three-phase voltage sag.

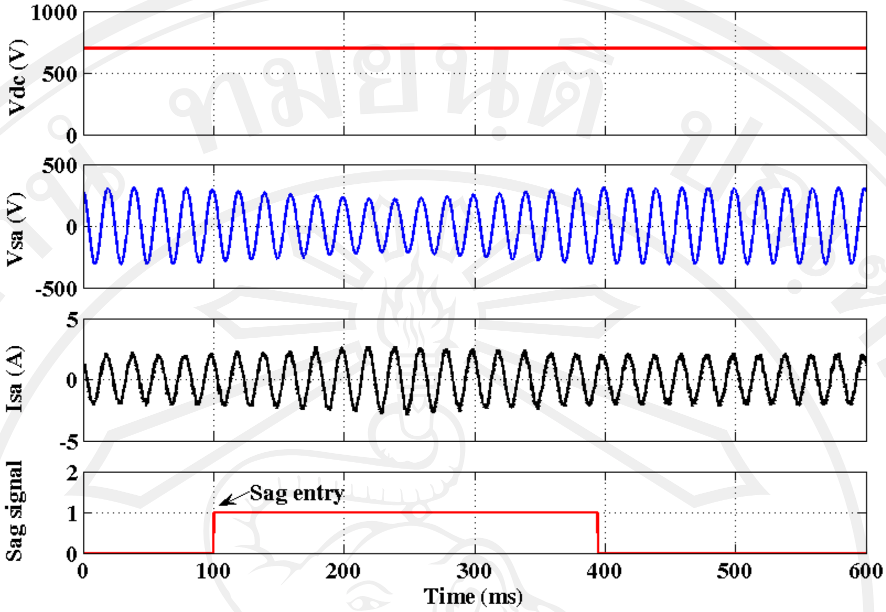
It can be seen that the back-to-back converter is trying to regulate the DC-link voltage by gradual increasing the sinusoidal wave input current of back-to-back converter during voltage sag occurs (due to constant output power, when the grid voltage decreases, the input current must be increased).

It can be noticed that the converter input current is controlled to be sinusoidal wave (i.e. low total harmonic distortion) and the input power factor is maintained to be nearly unity (input voltage and input current are in phase) which caused less power quality problem even the load is non-linear load (rectifier load). Therefore, the other electronic and electric equipments or capacitor banks which are connected in the same PCC (point of common coupling) will not experience the harmonic problem due to proposed voltage sag compensator. The operation of the proposed voltage sag compensator will not produce the power quality problem to the electrical power distribution systems.

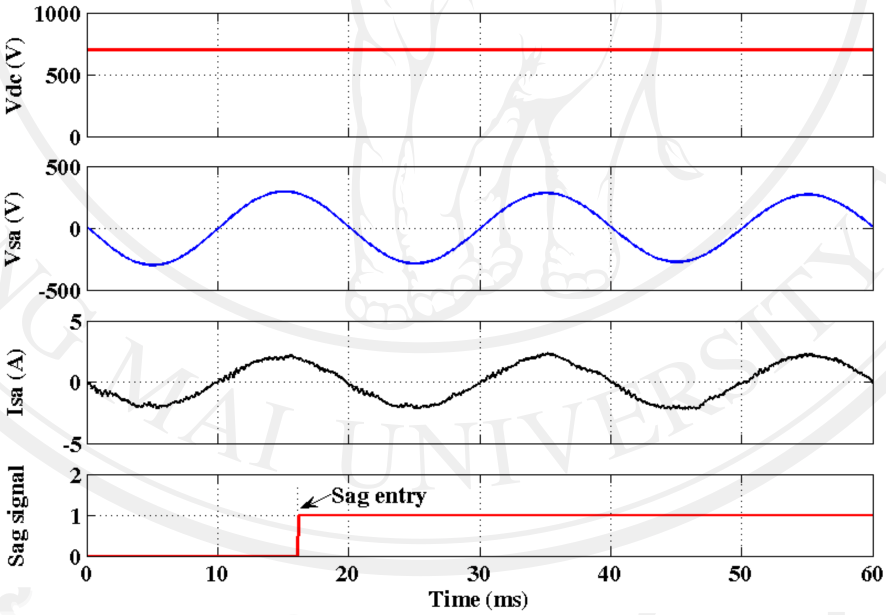
With replacing the rectifier load by inductive load, the input side waveforms of back-to-back converter under three-phase voltage sag are shown in Figure 5.9.

It can be noticed that the controlling of DC-link voltage is very good as well. The converter input current is still controlled to be sinusoidal wave and unity power factor.

It can be obviously seen that the proposed voltage sag compensator can be operated with any type of load such as non linear loads and inductive loads (the operation of proposed voltage sag compensator with the resistive loads are not presented in this thesis since they are very basic loads). Most of sensitive loads are



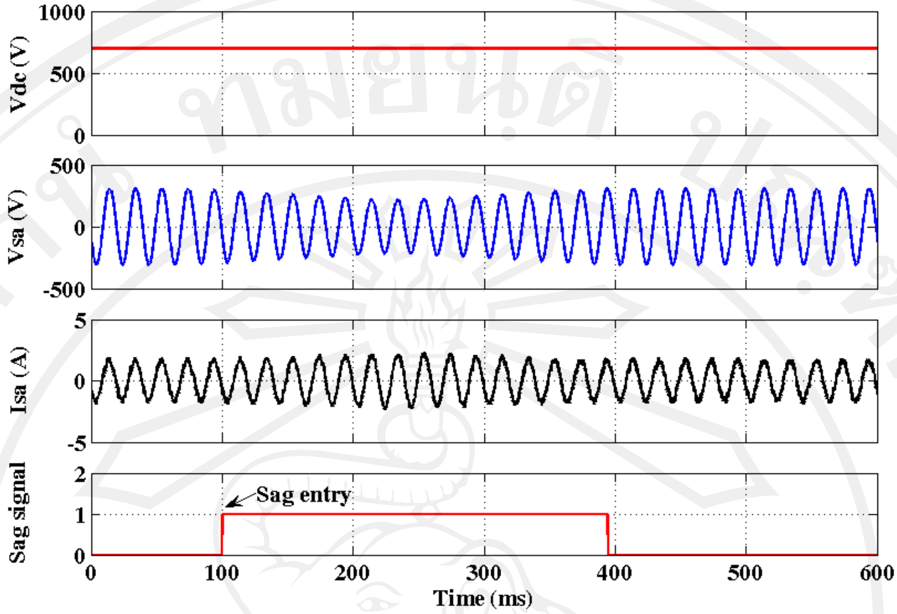
(a)



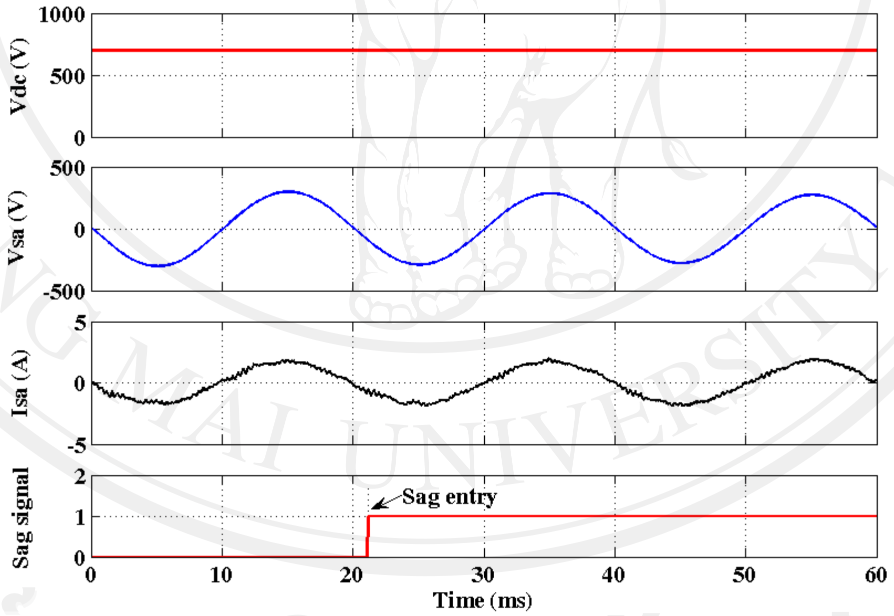
(b)

Figure 5.8 Simulation results of back-to-back converter operation at input side under three-phase voltage sag and rectifier load. (a) Normal view. (b) Extended view.

non linear loads (rectifier loads), such as variable speed drives, automation controllers and inductive loads which as induction motor, magnetic contactors and relays.



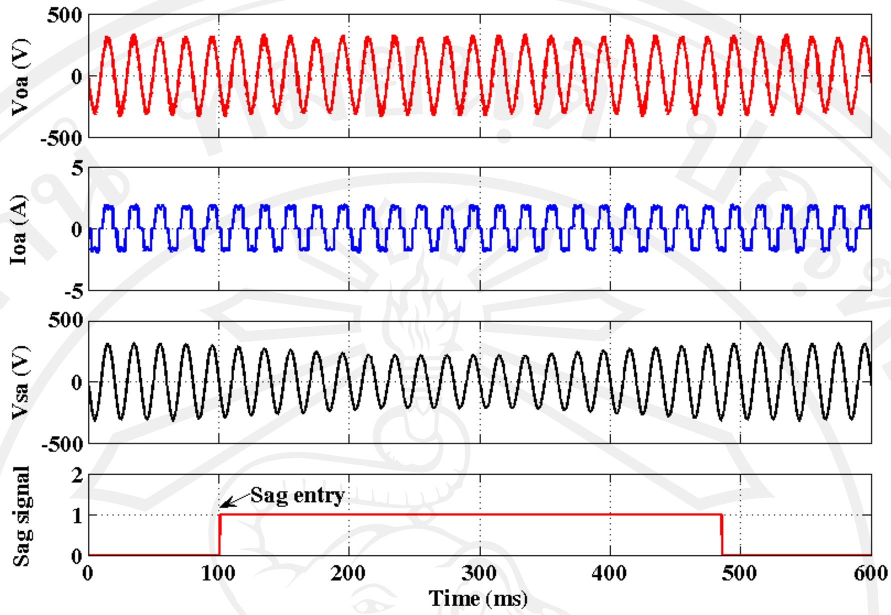
(a)



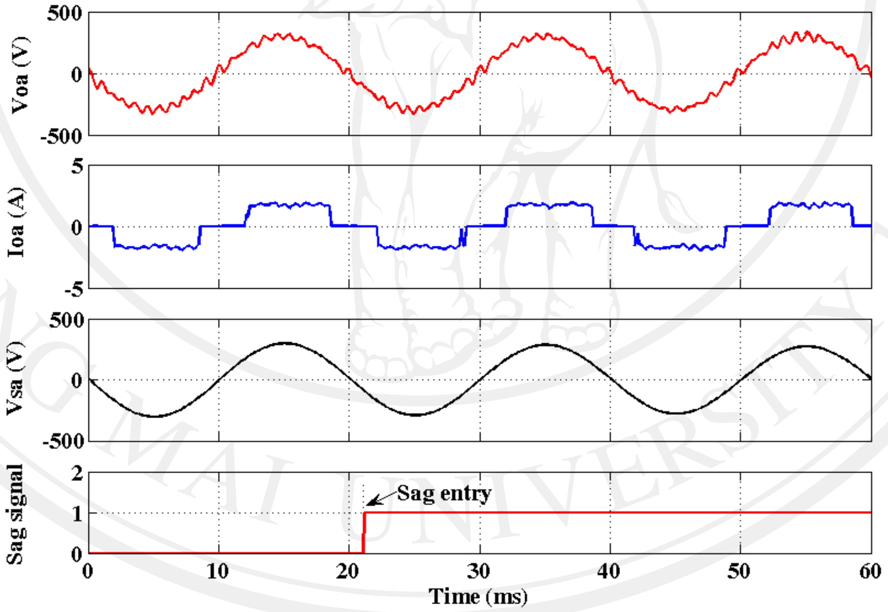
(b)

Figure 5.9 Simulation results of back-to-back converter operation at input side under three-phase voltage sag and inductive load. (a) Normal view. (b) Extended view.

The output side measurement of back-to-back converter in case of rectifier load is shown in Figure 5.10. It can be seen that the load voltage is tightly regulated under voltage sag. In other words, the load voltage is not affected from deviation of the grid



(a)

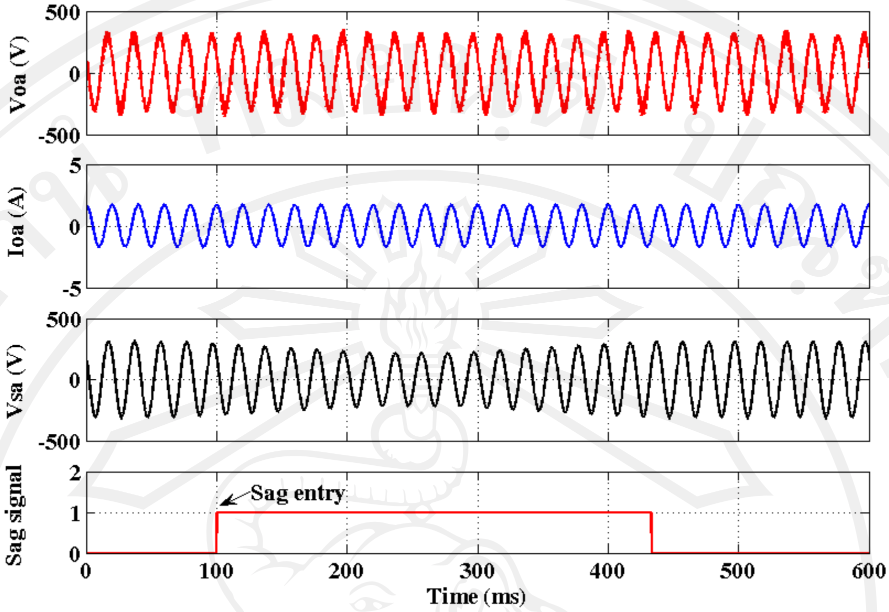


(b)

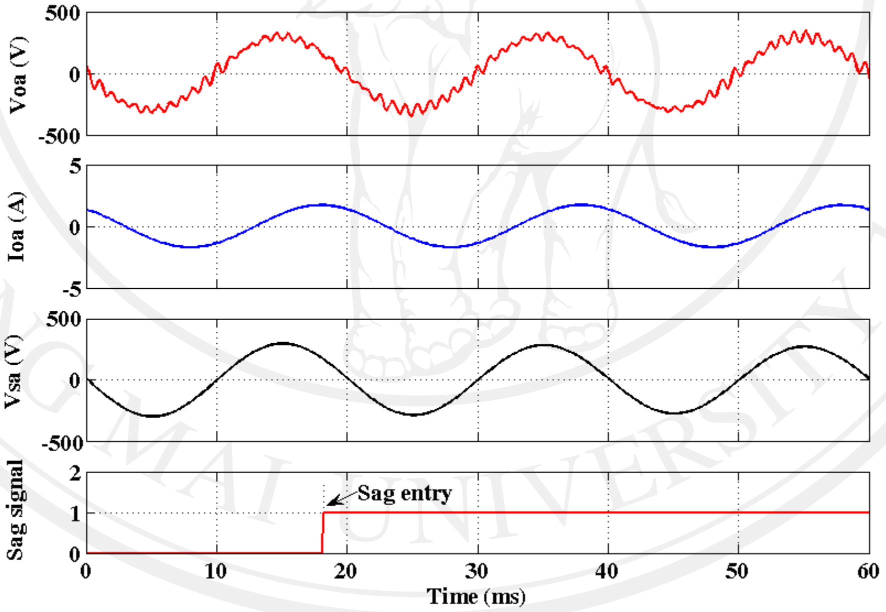
Figure 5.10 Simulation results of back-to-back converter operation at output side under three-phase voltage sag and rectifier load. (a) Normal view. (b) Extended view.

voltage. This is because of the constant DC-link voltage during voltage sag period. The load voltage THD of Figure 5.6 (b) is 6.5%.

Figure 5.11 illustrates the output side measurement in case of inductive load. The load voltage is still constant when voltage sag occurs. Thus the load is not affected against the voltage sag.



(a)



(b)

Figure 5.11 Simulation results of back-to-back converter operation at output side under three-phase voltage sag and inductive load. (a) Normal view. (b) Extended view.

5.5.2.2 Load compensation

In this section, the load compensation of the proposed voltage compensation system was simulated under three-phase voltage sag. The load types are three-phase rectifier load and three-phase star inductive load. It can be noticed that there is no star point in three-phase rectifier load then the measured voltage has to be line voltage.

The measured parameters consist of converter line input voltage (V_{sab}), load current (I_{oa}), and load phase voltage (V_{oab}), respectively, as shown in Figure 5.12.

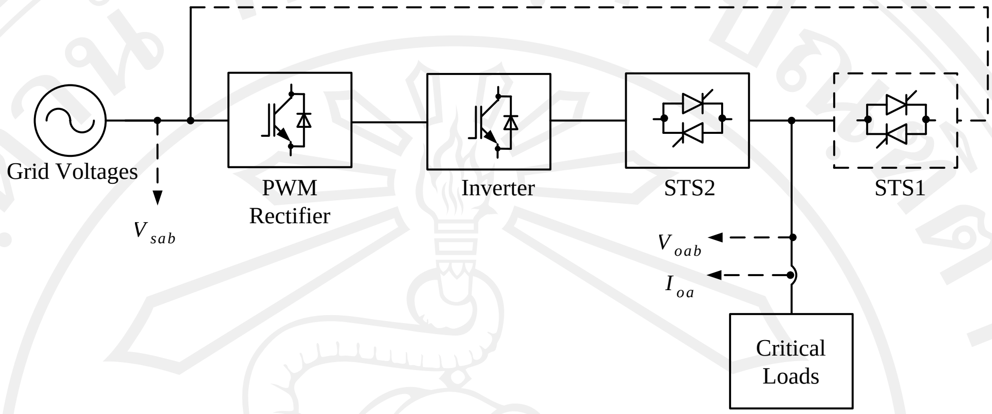


Figure 5.12 Simulation setup for load compensated operation.

The main objective of this simulation is to show the performance of the proposed voltage sag compensator when the voltage sag occurs in the condition of various loads (non-linear load and inductive load).

In this simulation, the operations of back-to-back are shown in the period of 600 ms or 30 cycles and the extended view of waveforms (3 cycles) around grid voltage deviation period are plotted to show the detail of waveforms.

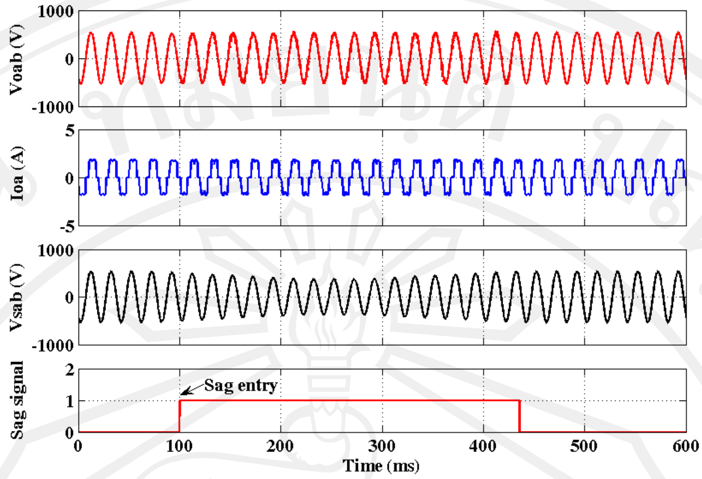
To avoid the short circuit problem in practical case, the 300-ms dead time of STS is utilized. This dead time is used to ensure the completion of the commutation process of thyristor-based STS.

The operation waveforms of the proposed system for load compensation with the rectifier load are illustrated in Figure 5.13 to verify the performance of the proposed voltage sag compensation system under voltage sag.

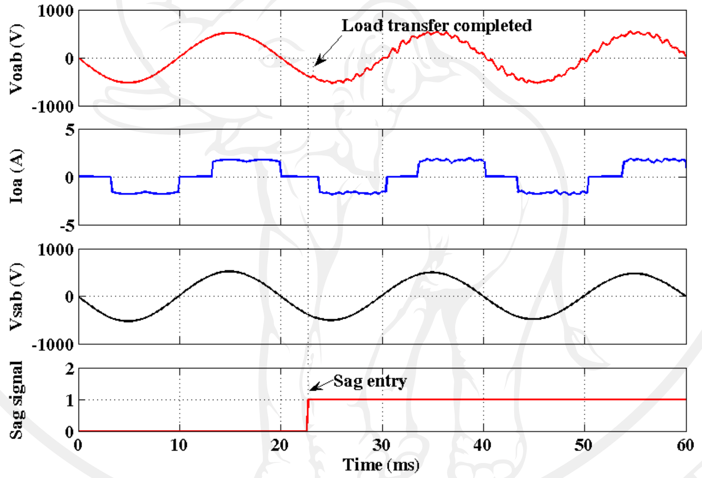
It can be noticed that the load voltage is also immediately compensated whenever the voltage sag occurs and the transition from the grid voltages to the back-to-back converter is realized in a seamless fashion as shown in Figure 5.13(b). When the voltage sag is cleared, the transition from the back-to-back converter to the grid voltages is also realized in a seamless fashion as shown in Figure 5.13(c).

As mentioned in chapter 4, for the rectifier load, the load current and load voltage are always in the same polarity. Therefore, load transferring process can be promptly initiated by STS whenever the sag signal is active.

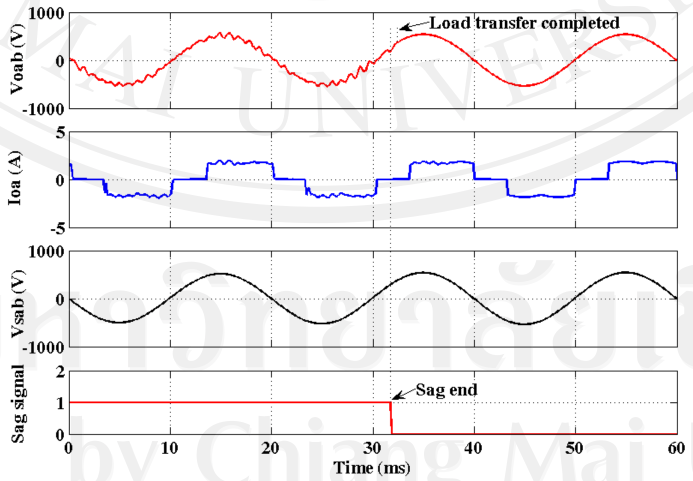
In Figure 5.14, the proposed voltage sag compensation system operates under 0.7-pu three-phase voltage sag with inductive load is illustrated. It can be noticed that once the voltage sag occurs then the load voltage is immediately compensated. The load transition from the grid voltages to the back-to-back converter is performed without any noticeable glitch at the load voltage as shown in Figure 5.14(b). The load voltage is also almost constant throughout the sag period. In Figure 5.14(c), it can be seen that the transition from the back-to-back converter to the grid voltages is also performed without any noticeable glitch.



(a)

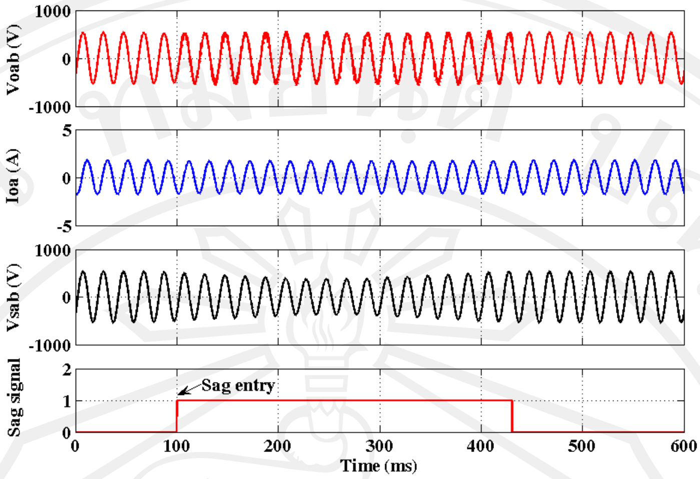


(b)

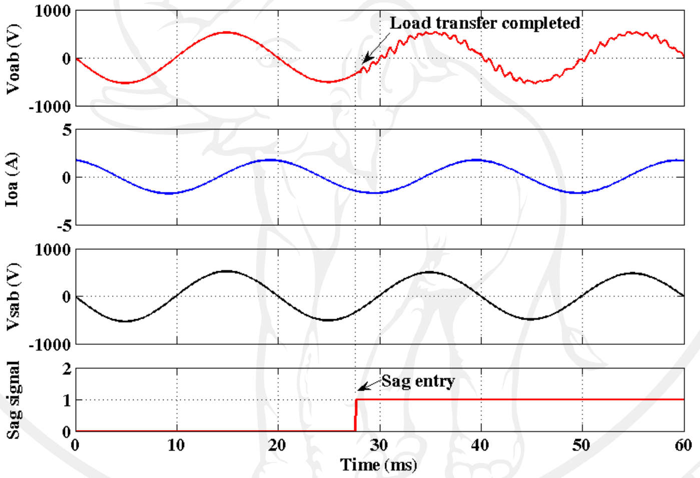


(c)

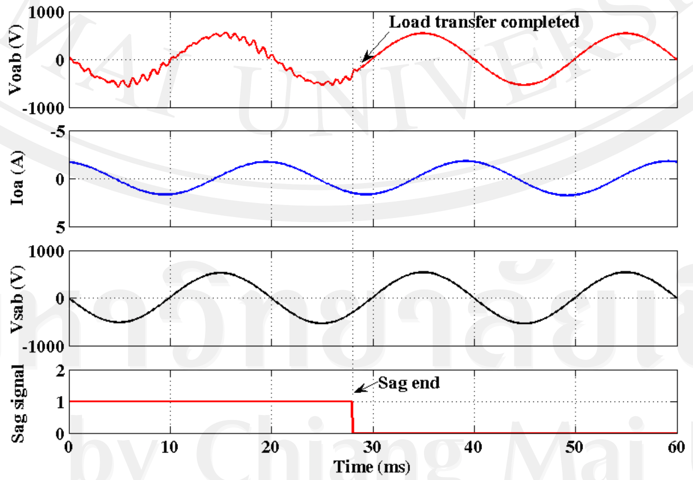
Figure 5.13 Simulation results of load compensation under three-phase voltage sag and rectifier load. (a) Normal view. (b) Extended view (sag entry). (c) Extended view (sag end).



(a)



(b)



(c)

Figure 5.14 Simulation results of load compensation under three-phase voltage sag and inductive load. (a) Normal view. (b) Extended view (sag entry). (c) Extended view (sag end).

It can be seen from Figure 5.14 that the load transferring process can be immediately executed by STS when the sag signal is active. This is because of the same polarity of load voltage and load current (t3 stage) as mentioned in chapter 4.

5.5.3 Experimental results

In this section, the experimental results are shown. The experimentation consists of back-to-back converter operation during sag, and load compensation during sag. Load types in this experimentation are three-phase rectifier load and inductive load to show the performance of proposed voltage sag compensation system.

5.5.3.1 Back-to-back converter operation

In this section, the operation of back-to-back converter was experimented. The measurements are determined at the input side and output side of back-to-back converter as shown in Figure 5.15. The measured parameters of input side consist of DC-link voltage (V_{dc}), converter phase input voltage (V_{sa}), and converter input current (I_{sa}).The measured parameters of output side consist of load voltage (V_o), converter output current (I_{oa}), and converter phase input voltage (V_{sa}), respectively. In this experimentation, the operations of back-to-back are shown in the period of 600 ms or 30 cycles.

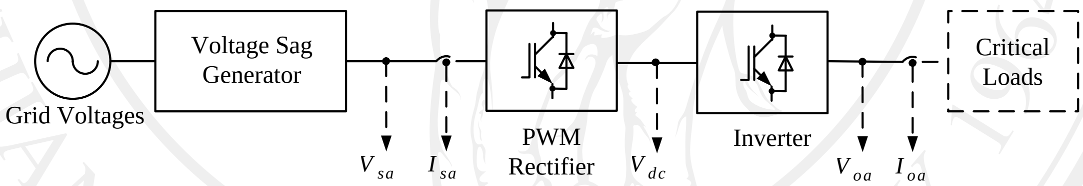


Figure 5.15 Experimental setup for back-to-back converter operation.

Figure 5.16 shows the waveforms of back-to-back converter at input side under three-phase voltage sag and rectifier load. It can be seen that the controller is trying to regulate the DC-link voltage by gradual increasing the input current of back-to-back converter during voltage sag occurs.

It can be noticed from Figure 5.16 (b) that the converter input current is controlled to be sinusoidal wave. Therefore, a low total harmonic distortion can be the result of this sinusoidal wave input current. Besides, the controlled input current and input voltage are in phase. Thus, a high power factor (near unity) is the result from this subject. Both of advantages (the low harmonic distortion and the high power factor) are leading to the less power quality problem even the load is non-linear load (rectifier load).

In Figure 5.17, the waveforms of back-to-back converter at the input side under three-phase voltage sag and inductive load are presented. It can be seen that the DC-link voltage is regulated to the set point value (700Vdc) during voltage sag occurs. The input current is still controlled to be sinusoidal wave and is in phase with input voltage. Therefore, the low total harmonic distortion and the high power factor can be the result of these subjects.

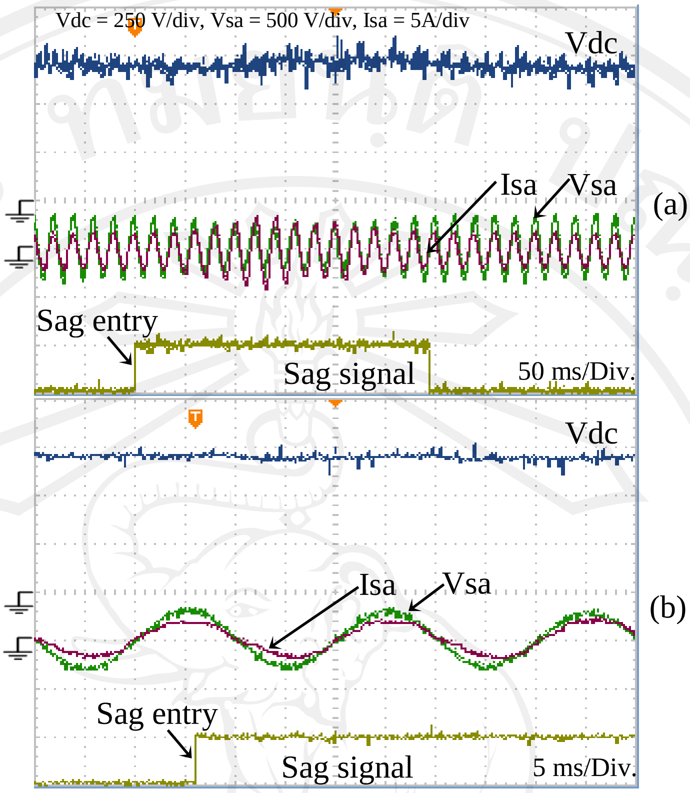


Figure 5.16 Experimentation results of back-to-back converter operation at input side under three-phase voltage sag and rectifier load. (a) Normal view. (b) Extended view.

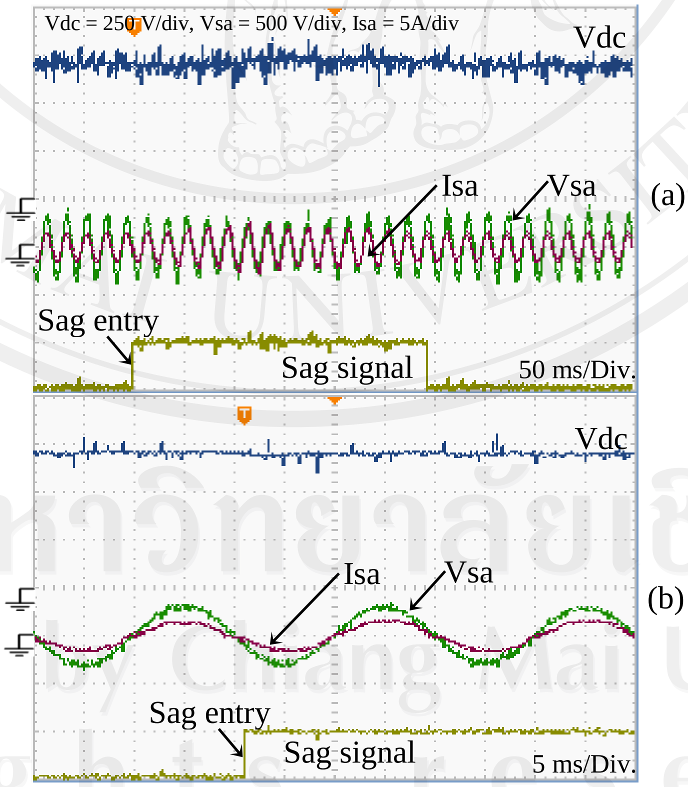


Figure 5.17 Experimentation results of back-to-back converter operation at input side under three-phase voltage sag and inductive load. (a) Normal view. (b) Extended view.

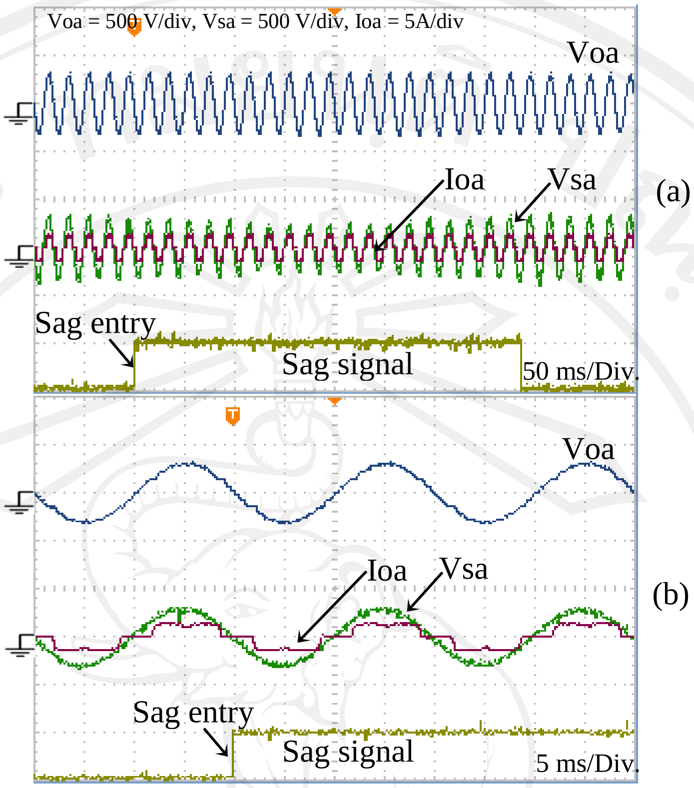


Figure 5.18 Experimentation results of back-to-back converter operation at output side under three-phase voltage sag and rectifier load. (a) Normal view. (b) Extended view.

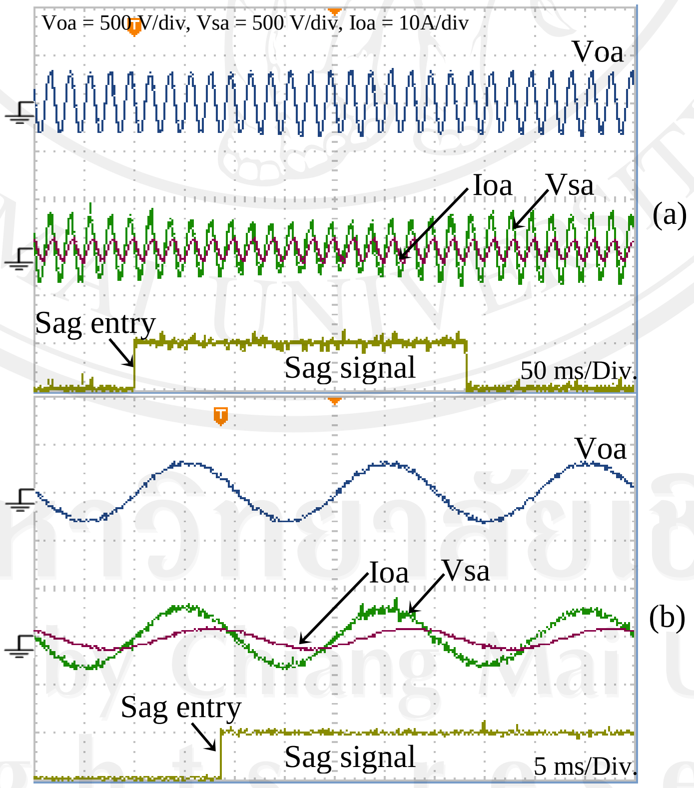


Figure 5.19 Experimentation results of back-to-back converter operation at output side under three-phase voltage sag and inductive load. (a) Normal view. (b) Extended view.

It can be clearly seen that the proposed voltage sag compensator can work with any type of load (such as non linear loads and inductive loads) without interference the electrical power distribution systems.

Figure 5.18 and 5.19 show the waveforms of back-to-back converter at the output side with the rectifier load and inductive load respectively. It can be seen that the load voltage (or the output voltage of back-to-back converter) are controlled during voltage sag period. Thus, the load will not affected by voltage deviation and continuous operation of load is achieved.

5.5.3.2 Load compensation

In this section, load compensation of proposed voltage compensation system was experimented under three-phase voltage sag. The load types are three-phase star inductive load and three-phase rectifier load. The measured parameters consist of converter line input voltage (V_{sab}), load current (I_{oa}), and load phase voltage (V_{oab}), respectively.

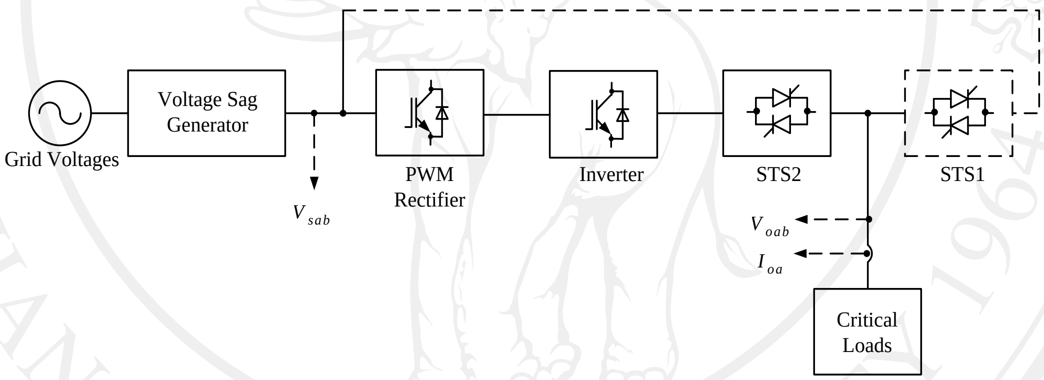


Figure 5.20 Experimental setup for load compensation.

The intention of this experimentation is to investigate the performance of the proposed voltage sag compensator during the voltage sag period in the condition of various loads (non-linear load and inductive load). This is the main goal of this research.

As mentioned in the simulation section, to avoid the short circuit problem of STS, the 300-ms dead time of STS is utilized.

The operation waveforms of the proposed voltage sag compensator for load compensation with rectifier load and inductive load are illustrated in Figure 5.21 and Figure 5.22, respectively.

In Figure 5.21, it can be noticed that the load voltage is also immediately compensated when the voltage sag occurs and the load transition from faulty grid voltage to the output of back-to-back converter is realized in a seamless fashion as shown in figure 5.21(b).

Case of inductive load is shown in Figure 5.23. The load transition from faulty grid voltage to the output of back-to-back converter is also realized in a seamless

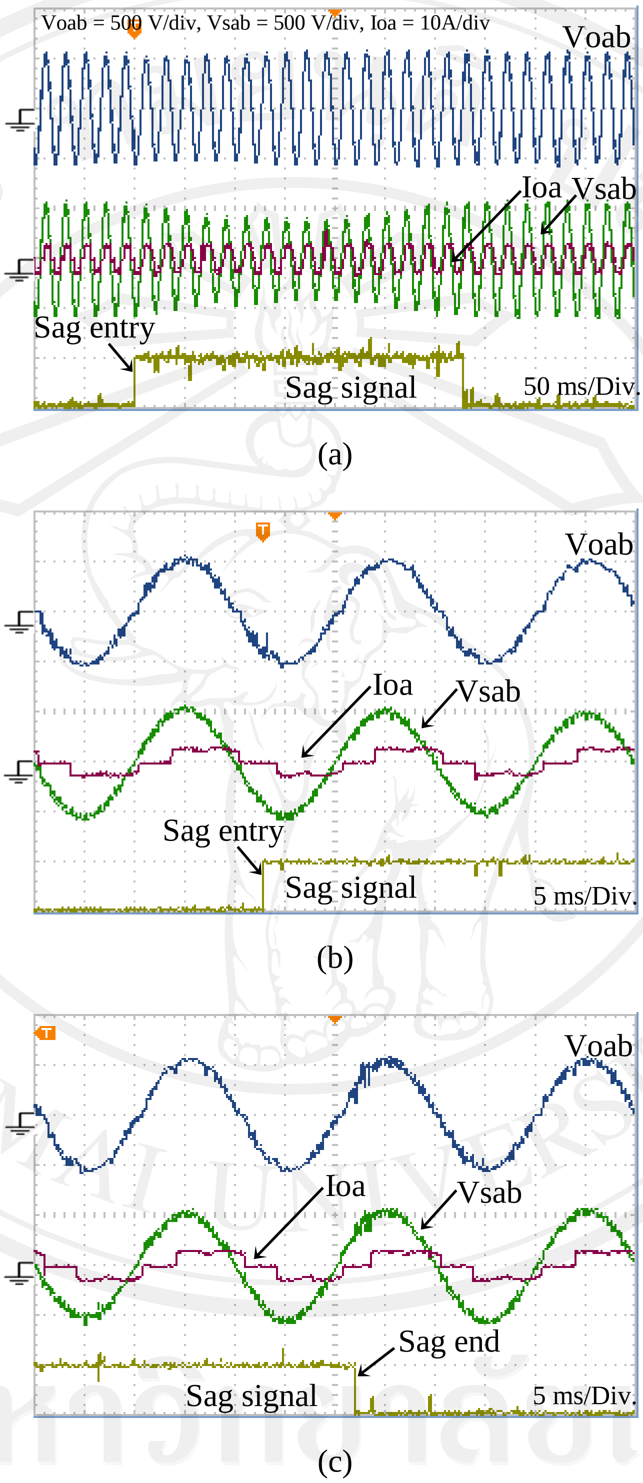


Figure 5.21 Experimentation results of load compensation under three-phase voltage sag and rectifier load. (a) Normal view. (b) Extended view (sag entry). (c) Extended view (sag end).

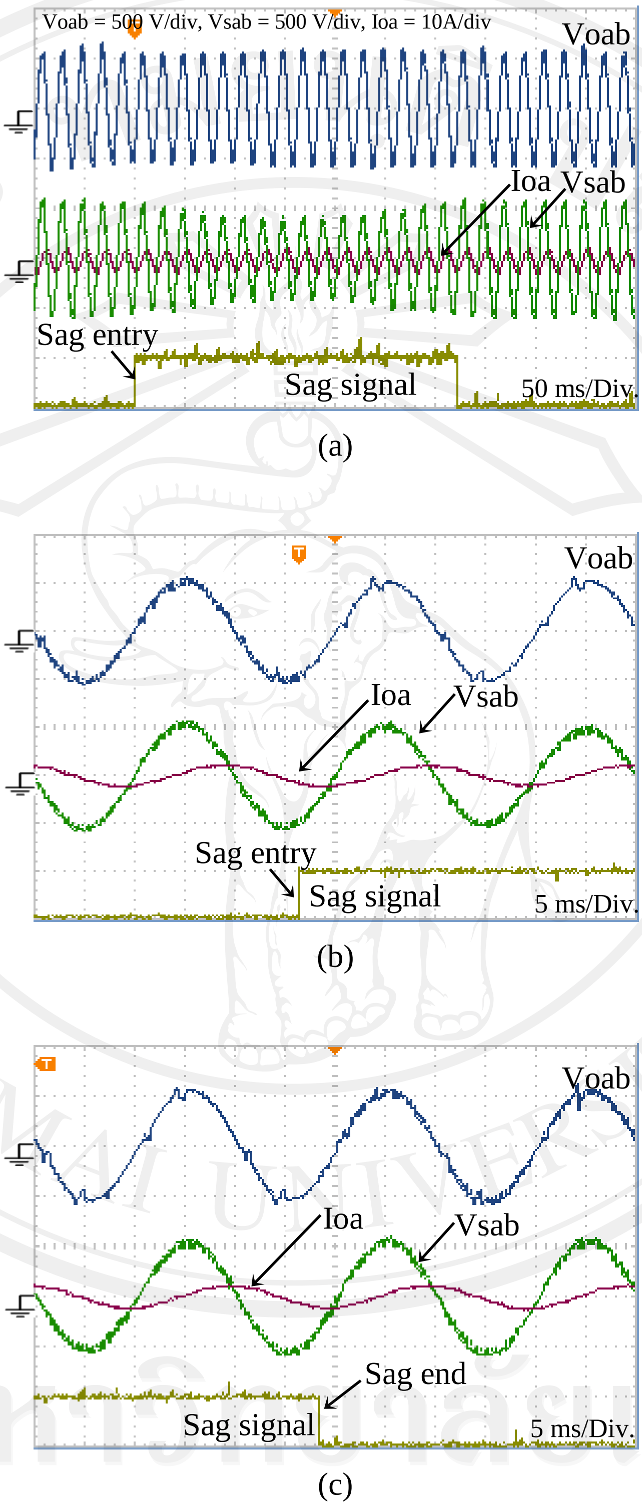


Figure 5.22 Experimentation results of load compensation under three-phase voltage sag and inductive load. (a) Normal view. (b) Extended view (sag entry). (c) Extended view (sag end).

fashion. It can be seen that the load voltage is regulated throughout the sag period i.e. voltage sag will not affect the load.

It can be seen from Figure 5.23 that due to the same polarity of load voltage and load current then the load transferring process can be immediately operated by STS.

5.6 Conclusions

In this chapter, the proposed voltage sag compensator is presented. The proposed voltage sag compensation system consists of 3 main parts 1) the voltage sag detection 2) static transfer switch (STS) and 3) back-to-back converter. The voltage sag detection is the first important part since it has to detect voltage sag events and initiate the next compensate processes as fast as possible. When the voltage sag is detected, STS is used for transferring the load from the grid voltage to the alternate supply voltage. Finally, the back-to-back converter is used to generate alternate supply voltage. It can be seen from the simulation and experimentation results that the load voltage can be regulated during sag period by using of the proposed voltage sag compensator (both of rectifier load and inductive load). The input current of the proposed system is controlled to be sinusoidal wave during sag cycles, i.e. a low harmonic distortion is obtained. Besides, the input current and the input voltage are in phase, i.e. a high power factor is achieved. Therefore, the less power quality problem can be result of these 2 issues.