CHAPTER 3

Three-Level Neutral Point Clamped Voltage Source Converter and Carrier Based Pulsewidth Modulation Technique

3.1 Introduction

Multilevel converter topologies have recently been increasingly applied in medium- and high-voltage, and medium- and high-power industrial applications, such as active power filters, static reactive power compensation, adjustable-speed drive, and renewable energy generation, due to advantages of high power rating, high quality output waveforms associated with reduced voltage/current harmonic distortions, low electromagnetic compatibility (EMC) concerns, lower common-mode voltage, lower switching losses, and higher efficiencies when compared to the conventional two-level voltage source converters [30]-[32].

Nowadays, there are three generally commercial classified topologies of multilevel converters in the literature as diode-clamped converters [33], [34], cascaded H-bridge converters [35]-[37], flying-capacitor converters [38], [39], and hybrid multilevel converters [40], whose classification is shown in Figure 3.1.

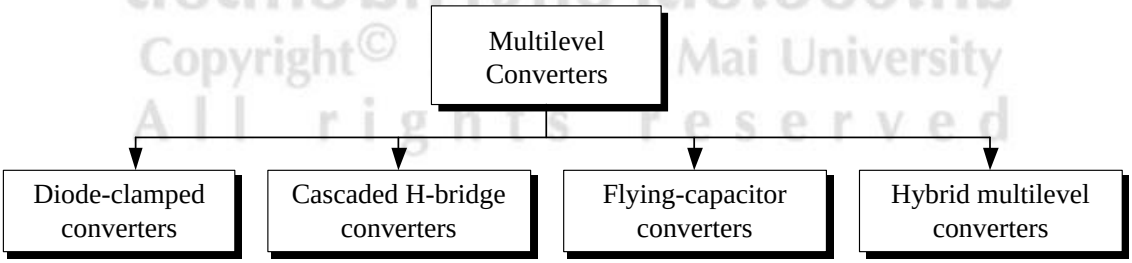


Figure 3.1 Classification of multilevel voltage source converter configurations.

This chapter describes the basic structure of three-level neutral-point-clamped (NPC) voltage source inverter (VSI) and presents simple modified unipolar carrier-based

pulsewidth modulation (CB-PWM) strategy. Analytical expressions for the relationship between modulation reference signals and output voltages are derived. The proposed modulation technique for the three-level NPC VSI includes the maximum and minimum of the three-phase sinusoidal reference voltages with zero-sequence voltage injection concept. The proposed modified CB-PWM strategy incorporates a novel method that requires only one triangular carrier wave for generating the gating pulses in three-level NPC VSI. It has the advantages of being simplifying the algorithm with no need of complex two/multi-carrier pulsewidth modulation or space vector modulation (SVM) and it is also simple to implement. The possibility of the proposed CB-PWM technique has been verified through computer simulation and experimental results.

3.2 Three-level neutral point clamped voltage source inverter

Among the various multilevel converter topologies, the most popular topology in high power industrial applications is the three-level neutral point clamped (NPC) voltage source inverter (VSI), which was proposed in 1981 by Nabae et al. [33], as shown in Figure 3.2. One advantage of the three-level NPC VSI topology is that the power switches and the dc-link capacitors have to endure only one-half of the dc-link voltage. As a result, the converter can deal with double voltage and power value than in a standard two-level VSI with the same switching frequency. However, the drawbacks of this topology are the higher number of power switches, which adds complexity to the modulation method. In addition, the voltage balance of the dc-link neutral point is required [34].

3.2.1 Three-level neutral point clamped voltage source inverter configuration

Figure 3.2 shows the simplified schematic of the power circuit of the three-level NPC VSI. It consists of twelve active switches, twelve anti-parallel-connected freewheeling diodes, six clamp diodes, and a split dc-link with series connected capacitors. For example, the inverter leg A is composed of four active switches S_{A1} to S_{A4} with four anti-parallel-connected freewheeling diodes D_{A1} to D_{A4}. The diodes connected to the neutral point Z, D_{ZA1} to D_{ZA2}, are the clamping diodes. On the dc-link side of the

inverter, the dc-link voltage capacitor is split into two, providing a neutral point.

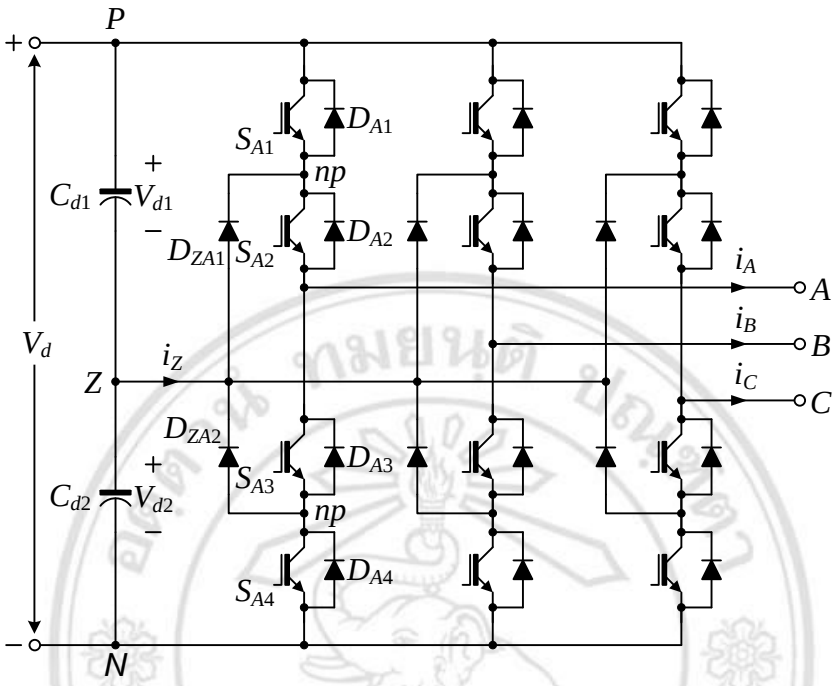


Figure 3.2 Simplified schematic of the power circuit of the three-level NPC VSI.

3.2.2 Switching states

The operating status of the switches in the three-level NPC VSI can be represented by switching states shown in Table 3.1, where k denotes one of the three-phase A, B, or C, and v_{kZ} denotes the each output pole voltage. This voltage has three possible values, namely $V_d/2$, 0, and $-V_d/2$. The switching state 'P' denotes that in each phase, two switches, S_{k1} and S_{k2}, are on and the output pole voltage v_{kZ}, which is the voltage terminal with respect to the neutral point Z, is $V_d/2$. The switching state 'N' implies that the lower two switches (S_{k3} and S_{k4}) conduct and lead to $v_{kZ} = -V_d/2$. The switching state 'O' signifies that the switches S_{k2} to S_{k3} are on. The output voltage is clamped to zero through the clamping diodes, D_{ZA1} to D_{ZA2}. It can be observed from Table 3.1 that two switches of each phase are closed whilst the other two are opened. In other words, switches S_{k1} and S_{k3} operate in a complementary manner. With one switches on, the other must

be off. Similarly, S_{k2} and S_{k4} are a complementary pair as well. In each leg, three valid switching states are available to generate three voltage levels on the output pole voltage.

Table 3.1 Switching states and pole voltages of a three-level neutral point clamped voltage source inverter

Switching Symbols	Switching States				Pole Voltage
	S_{k1}	S_{k2}	S_{k3}	S_{k4}	v_{kZ}
P	ON	ON	OFF	OFF	$V_d / 2$
O	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	$-V_d / 2$

Referring to Figure 3.2 and switching states, each phase of the inverter can give the output with three different values. Thus, there exist totally 27 (3^3) switching states consisting of 24 nonzero voltage vectors and three zero voltage vectors possible combinations of output voltages. By drawing these 27 vector space voltages in the stationary reference frame, three instantaneous voltage hexagons in space vector plan are distinguished as illustrated in Figure 3.3. According to their length, the voltage vectors can be divided into four groups as zero vectors ($\vec{v}_0, \vec{v}_7, \vec{v}_{14}$), small vectors ($\vec{v}_1 - \vec{v}_6$ and $\vec{v}_8 - \vec{v}_{13}$), medium vectors ($\vec{v}_{15} - \vec{v}_{20}$), and large vectors ($\vec{v}_{21} - \vec{v}_{26}$).

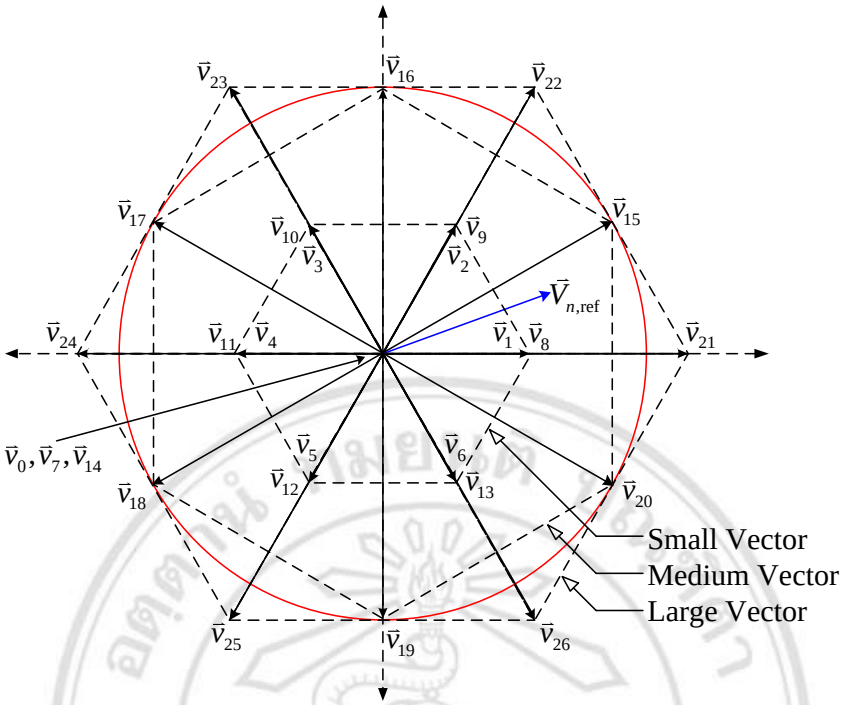


Figure 3.3 Space vector voltages diagram of the three-level NPC VSI.

3.3 Carrier-based pulsewidth modulation technique

The objective of this section is to present the proposed carrier-based pulse width modulation strategy, which evaluates performance of the three-level NPC VSI of Figure 3.2.

3.3.1 Principle of the proposed CB-PWM strategy

Numerous studies about the CB-PWM strategy for the three-level NPC VSI have been published [41], which assists to understand the proposed method in this paper. From their results, it is widely known that the addition of a zero-sequence voltage v_0^* selected as (3.1) to the three-phase sinusoidal reference voltages v_A^*, v_B^*, v_C^* in (3.2) locates the non-zero voltage vectors in the center of a sampling period [42]-[44]. It provides an optimum switching sequence by which it has some advantages, such as lower harmonic distortion and higher available modulation index m_a, compared with the SPWM technique. The zero-sequence voltage v_0^* can be generated as,

$$v_0^* = -\frac{\max\left(v_A^*, v_B^*, v_C^*\right) + \min\left(v_A^*, v_B^*, v_C^*\right)}{2}. \tag{3.1}$$

In the traditional modulation method, the three-phase reference voltages including the zero-sequence voltage v_0^* for generating the non-sinusoidal three-phase reference voltages $v_{A,0}^*, v_{B,0}^*, v_{C,0}^*$ which can be described by,

$$\begin{cases} v_{A,0}^* = v_A^* + v_0^*, \\ v_{B,0}^* = v_B^* + v_0^*, \\ v_{C,0}^* = v_C^* + v_0^*, \end{cases} \tag{3.2}$$

where the sinusoidal three-phase reference voltages, v_A^*, v_B^*, v_C^*, are given by,

$$\begin{cases} v_A^* = m_a \sin\left(\omega_s t\right), \\ v_B^* = m_a \sin\left[\omega_s t - \left(2\pi/3\right)\right], \\ v_C^* = m_a \sin\left[\omega_s t + \left(2\pi/3\right)\right], \end{cases} \tag{3.3}$$

where the normalized modulation index m_a controls the voltage magnitude and has a range of 0 to 1.0.

In (3.3), $\omega_s t$ is the inverter electrical position which may be related to a desired fundamental frequency f_1 of output voltages by,

$$\omega_s t = 2\pi f_1 t. \tag{3.4}$$

The traditional CB-PWM strategy takes the instantaneous average of the maximum and minimum of the three-phase reference voltages and adds this value from each of the sinusoidal three-phase reference voltages to obtain the modulation waveforms. The addition of this zero-sequence voltage continuously centers all of the three reference waveforms in the carrier band, which is similar to the CB-PWM conventional two-level VSI. The CB-PWM technique can only be used for three-phase three-wire system, and it enables the modulation index to be increased by 15.5% before over-modulation.

In the traditional CB-PWM strategy, the three-phase sinusoidal reference voltages including the zero-sequence voltage v_0^* for generating the reference voltages of phase leg voltages. The proposed CB-PWM strategy is a generalized method that uses the effective three-phase sinusoidal reference voltage and the maximum and minimum of the three reference voltages.

Two new variables of the modified reference voltage in the proposed CB-PWM strategy are obtained through double reference voltages v_{kP}^* and v_{kN}^* ($k \in A,B,C$) for each phase. The modified reference voltages $v_{A,M}^*, v_{B,M}^*, v_{C,M}^*$ are derived as follows:

$$\begin{cases} v_{A,M}^* = v_{AP}^* + v_{AN}^*, \\ v_{B,M}^* = v_{BP}^* + v_{BN}^*, \\ v_{C,M}^* = v_{CP}^* + v_{CN}^*, \end{cases} \tag{3.5}$$

where $v_{AP}^*, v_{BP}^*, v_{CP}^*$ are the positive reference voltages and $v_{AN}^*, v_{BN}^*, v_{CN}^*$ are the negative reference voltages of the modified reference voltage v_k^*, respectively.

The positive reference voltages take the minimum of the three-reference voltages and subtract this value from each of the three-phase sinusoidal reference voltages, which can be expressed as,

$$\begin{cases} v_{AP}^* = \dfrac{v_A^* - \min\left(v_A^*, v_B^*, v_C^*\right)}{2}, \\ v_{BP}^* = \dfrac{v_B^* - \min\left(v_A^*, v_B^*, v_C^*\right)}{2}, \\ v_{CP}^* = \dfrac{v_C^* - \min\left(v_A^*, v_B^*, v_C^*\right)}{2}, \end{cases} \tag{3.6}$$

Similar to (3.6), the negative reference voltages takes the maximum of the three-reference voltages and subtract this value from each of the three-phase sinusoidal reference voltages,

$$\begin{cases} v_{AN}^{*} = \text{sgn}\left[\dfrac{v_A^{*} - \max\left(v_A^{*}, v_B^{*}, v_C^{*}\right)}{2} + \delta\right], \\ v_{BN}^{*} = \text{sgn}\left[\dfrac{v_B^{*} - \max\left(v_A^{*}, v_B^{*}, v_C^{*}\right)}{2} + \delta\right], \\ v_{CN}^{*} = \text{sgn}\left[\dfrac{v_C^{*} - \max\left(v_A^{*}, v_B^{*}, v_C^{*}\right)}{2} + \delta\right], \end{cases} \tag{3.7}$$

where sign function (sgn) is defined by +1 or -1, and $\delta \in \{0,1\}$.

Combining (3.6) and (3.7), the modified reference voltages, $v_{A,M}^{*}, v_{B,M}^{*}, v_{C,M}^{*}$ within the maximum and minimum of the three reference voltages, is calculated as,

$$\begin{cases} v_{A,M}^{*} = \left[\dfrac{v_A^{*} - \min\left(v_A^{*}, v_B^{*}, v_C^{*}\right)}{2}\right] + \text{sgn}\left[\dfrac{v_A^{*} - \max\left(v_A^{*}, v_B^{*}, v_C^{*}\right)}{2} + \delta\right], \\ v_{B,M}^{*} = \left[\dfrac{v_B^{*} - \min\left(v_A^{*}, v_B^{*}, v_C^{*}\right)}{2}\right] + \text{sgn}\left[\dfrac{v_B^{*} - \max\left(v_A^{*}, v_B^{*}, v_C^{*}\right)}{2} + \delta\right], \\ v_{C,M}^{*} = \left[\dfrac{v_C^{*} - \min\left(v_A^{*}, v_B^{*}, v_C^{*}\right)}{2}\right] + \text{sgn}\left[\dfrac{v_C^{*} - \max\left(v_A^{*}, v_B^{*}, v_C^{*}\right)}{2} + \delta\right]. \end{cases} \tag{3.8}$$

3.3.2 Output voltages synthesis

The main purposes of a CB-PWMs strategy of a three-level NPC VSI are to synthesize the desired output voltages and to verify the modified duty cycles. The output pole voltages v_{kZ}, which is the voltage at terminal k with respect to the neutral point Z of Figure 3.2, can be expressed as,

$$\begin{cases} v_{AZ} = \dfrac{V_d}{2}\left\{\left[\dfrac{v_A^* - \min\left(v_A^*, v_B^*, v_C^*\right)}{2}\right] + \operatorname{sgn}\left[\dfrac{v_A^* - \max\left(v_A^*, v_B^*, v_C^*\right)}{2} + \delta\right]\right\}, \\ v_{BZ} = \dfrac{V_d}{2}\left\{\left[\dfrac{v_B^* - \min\left(v_A^*, v_B^*, v_C^*\right)}{2}\right] + \operatorname{sgn}\left[\dfrac{v_B^* - \max\left(v_A^*, v_B^*, v_C^*\right)}{2} + \delta\right]\right\}, \\ v_{CZ} = \dfrac{V_d}{2}\left\{\left[\dfrac{v_C^* - \min\left(v_A^*, v_B^*, v_C^*\right)}{2}\right] + \operatorname{sgn}\left[\dfrac{v_C^* - \max\left(v_A^*, v_B^*, v_C^*\right)}{2} + \delta\right]\right\}, \end{cases} \quad (3.9)$$

where V_d is the dc-link voltage.

Form the above equations, these output pole voltages v_{AZ}, v_{BZ}, v_{CZ} are determined by the modified reference voltages $v_{A,M}^*, v_{B,M}^*, v_{C,M}^*$, directly. In the linear modulation index range, if the peak value of the line-to-line voltage is $\sqrt{3} m_a V_d / 2$, the instantaneous value of the output line-to-line voltages v_{AB}, v_{BC}, v_{CA} can be expressed as,

$$\begin{cases} v_{AB} = v_{AZ} - v_{BZ} = \dfrac{\sqrt{3} m_a V_d}{2} \sin\left[\omega_s t + (\pi / 6)\right], \\ v_{BC} = v_{BZ} - v_{CZ} = \dfrac{\sqrt{3} m_a V_d}{2} \sin\left[\omega_s t - (\pi / 2)\right], \\ v_{CA} = v_{CZ} - v_{AZ} = \dfrac{\sqrt{3} m_a V_d}{2} \sin\left[\omega_s t + (5\pi / 6)\right], \end{cases} \quad (3.10)$$

In the linear modulation range, (3.10), the output line-to-line voltages are equal to or less than dc-link voltage V_d. Therefore, if a three-phase balanced voltage is to be synthesized using CB-PWM scheme describe above. The modulation index is defined as,

$$m_a = \frac{2\hat{V}_{kZ,1}}{V_d}, \quad (3.11)$$

where $\hat{V}_{kZ,1}$ is the fundamental of output pole voltage (peak value), and the possible the modulation index in the linear range can be increased beyond m_a = 1.0 to the maximum modulation m_a = 1.15 before over-modulating.

Considering the inverter circuit shown in Figure 3.2, it can be seen that if the load is star-connected, the line-to-line voltages cannot clearly define the respective output phase voltages v_{An}, v_{Bn}, v_{Cn}, may be expressed in terms of the phase-to-ground voltages by,

$$\begin{cases} v_{An} = v_{AZ} - v_{nZ} = \frac{1}{3}\left(2v_{AZ} - v_{BZ} - v_{CZ}\right), \\ v_{Bn} = v_{BZ} - v_{nZ} = \frac{1}{3}\left(2v_{BZ} - v_{AZ} - v_{CZ}\right), \\ v_{Cn} = v_{CZ} - v_{nZ} = \frac{1}{3}\left(2v_{CZ} - v_{AZ} - v_{BZ}\right), \end{cases} \tag{3.12}$$

where v_{nZ} is the voltage between the neutral point of the load n and the neutral point of the dc-link capacitor Z, which can be calculated as,

$$v_{nZ} = \frac{1}{3}\left(v_{AZ} + v_{BZ} + v_{CZ}\right). \tag{3.13}$$

3.3.3 Calculation of duty cycles

A basic idea of this proposed CB-PWM strategy only requires the calculation of the independent duty cycles, which is to consider the output phase voltage in terms of the modified duty cycles d_A, d_B, d_C this may be described by,

$$\begin{cases} v_{AZ} = \frac{V_d}{2}\left(d_{AP} + d_{AN}\right) = \frac{V_d}{2} d_A, \\ v_{BZ} = \frac{V_d}{2}\left(d_{BP} + d_{BN}\right) = \frac{V_d}{2} d_B, \\ v_{CZ} = \frac{V_d}{2}\left(d_{CP} + d_{CN}\right) = \frac{V_d}{2} d_C, \end{cases} \tag{3.14}$$

where d_{AP}, d_{BP}, d_{CP} are positive duty cycles, and d_{AN}, d_{BN}, d_{CN} are negative duty cycles of the modified duty cycles.

From the above expressions, the equations show the relationships between effective duty cycles and output pole voltages. Commanded voltages are obtained by first defining a three-phase set of duty cycles which will be

offset so that they range from 0-100%. By solving (3.14), the modified duty cycles for output pole voltage, that is to divide the dc-link voltage, can be described as,

$$\begin{cases} d_A = d_{AP} + d_{AN} = \dfrac{2v_{AZ}}{V_d}, \\ d_B = d_{BP} + d_{BN} = \dfrac{2v_{BZ}}{V_d}, \\ d_C = d_{CP} + d_{CN} = \dfrac{2v_{CZ}}{V_d}, \end{cases} \tag{3.15}$$

where d_{kP}, d_{kN} are the modified upper and lower duty cycles, respectively.

The modified duty cycles defined by (3.15) can be compared to a set of single triangular carrier wave in order to produce a generalized switching state for the additional leg. Therefore, the algorithm can be simply implemented with a triangular carrier and the duty cycles calculation as shown in block diagram of Figure 3.4.

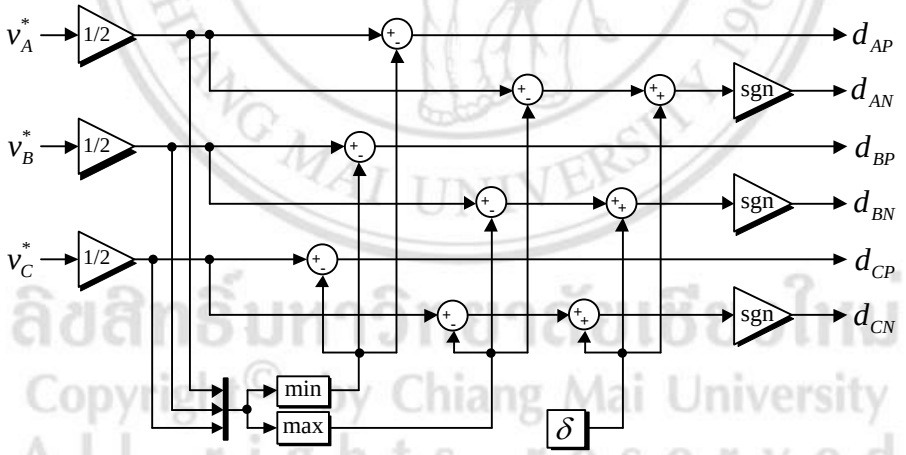


Figure 3.4 Proposed modified CB-PWM scheme for three-level NPC VSI.

The modified duty cycles of the proposed CB-PWM strategy are given in Figure 3.4. In Figure 3.5 (a), the original sinusoidal modulation signals v_A^*, v_B^*, v_C^* are used to generate the modified duty cycles in the proposed method. Figure 3.5 (b) shows the modified duty cycle waveforms d_{AP} and d_{AN} for leg A obtained from application of (3.6) and (3.7) to a sinusoidal

set of balanced modulation signals, which a line period, m_a = 1.0, sgn = +1, and δ = +1. The duty cycles for phase B and C are the same but phase shifted by $\pm 2\pi/3$. From these figures, it can be shown that the waveforms of the modified duty cycles in phase A comparative with single triangular wave, which are in the range 0 to 1. The expression for modified duty cycle d_{AN} is the same as d_{AP} but inverted and phase shifted of π radian.

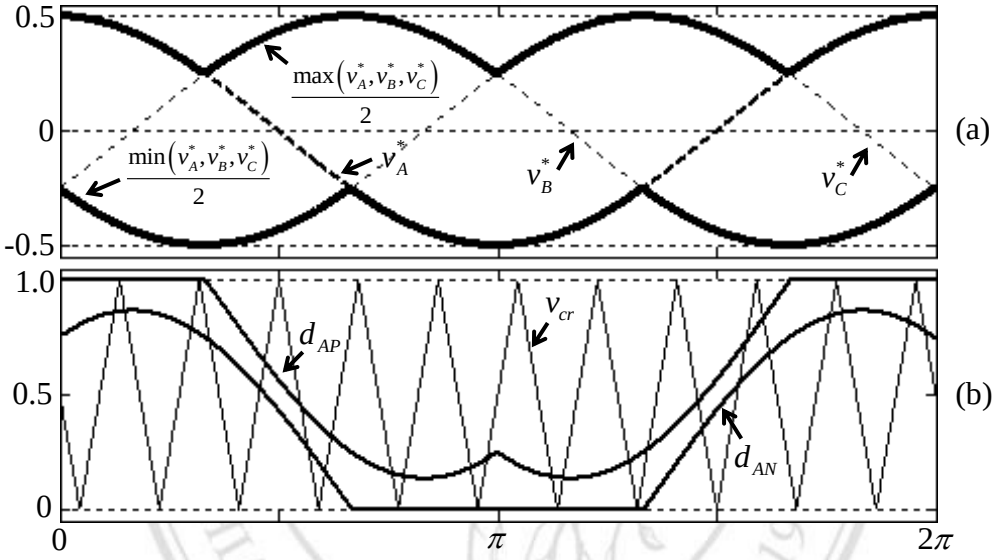


Figure 3.5 The modified duty cycles for leg A of the proposed CB-PWM strategy under the condition of m_a = 1.0, sgn = +1, and δ = +1.

For comparative purposes, the simulated duty cycles of the conventional CB-PWM strategies for three-level NPC VSI are illustrated in Figure 3.6 (a) and (b), which developed in [45] and [46], respectively. Figure 3.6 (a) shows the simulated duty cycles of the conventional CB-PWM 1 for leg A in the case that m_a = 1.0, sgn = +1, and δ = 0. From this result, it can be seen that the comparison of the duty cycles with two carriers, which consist of the upper and lower carriers (v_{cr1} and v_{cr2}). The positive signals will be compared with the upper carrier wave v_{cr1}, while the negative signal will be compared with the lower carrier wave v_{cr2}. In the same way, the upper duty cycles for double signals of conventional CB-PWM 2 with m_a = 1.0, sgn = -1, and δ = 0 are illustrated in Figure 3.6 (b). The results indicate that the

duty cycle d_{AP} is the same as d_{AN} but phase shifted of π radian. This method can also be implemented by using upper duty cycles but two phase shift carrier waves (v_{cr1} and v_{cr2}). The two carrier waves are the same amplitude and frequency, but out of phase.

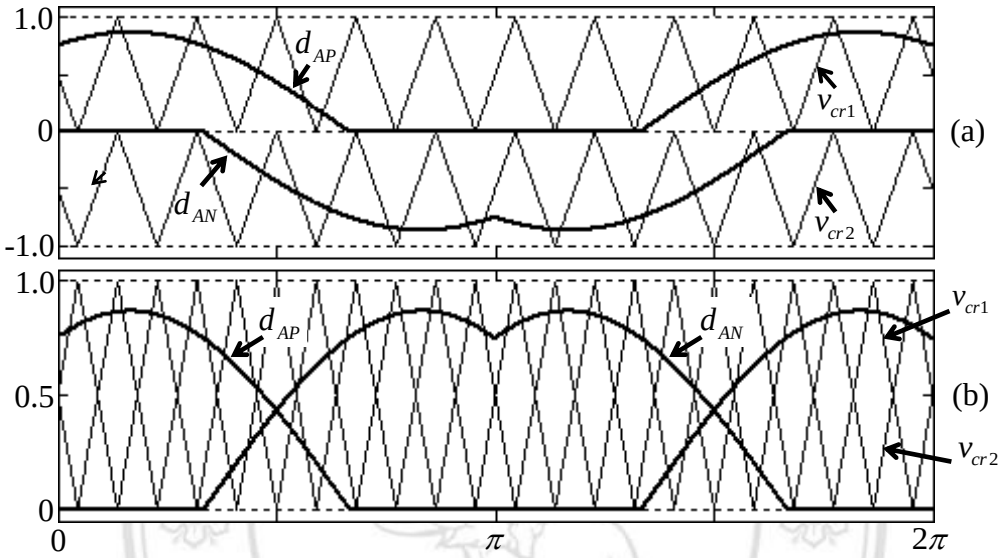


Figure 3.6 The modified duty cycles for leg A of the conventional CB-PWM strategies (a) Conventional CB-PWM 1: m_a =1.0, sgn = +1, and δ = 0 (b) Conventional CB-PWM 2: m_a = 1.0, sgn = -1, and δ = 0.

From the simulation duty cycles in Figure 3.5 (b) and Figure 3.6, all CB-PWM strategies give the same results for the output voltages, which are good performance. However, the proposed method is simple and easy to implement since the modified duty cycles utilized only one triangular carrier wave for generating the gating pulse in three-level NPC VSI.

3.4 Simulation results

In this section, some simulation results of the proposed method are presented. The modeling of the three-level NPC VSI using the proposed CB-PWM strategy has been implemented in Matlab/Simulink. The general conditions for the simulations are given as follows: the dc-link voltage V_d = 550 V, the dc-link capacitors C_{d1}, C_{d2} = 4700 μF, and the fundamental frequency f_1 = 50 Hz. The three-level NPC VSI feeds a 4-pole wye-connected induction motor, with nominal values of 1 kW, 1500 r/min, 220/380 V, 50 Hz.

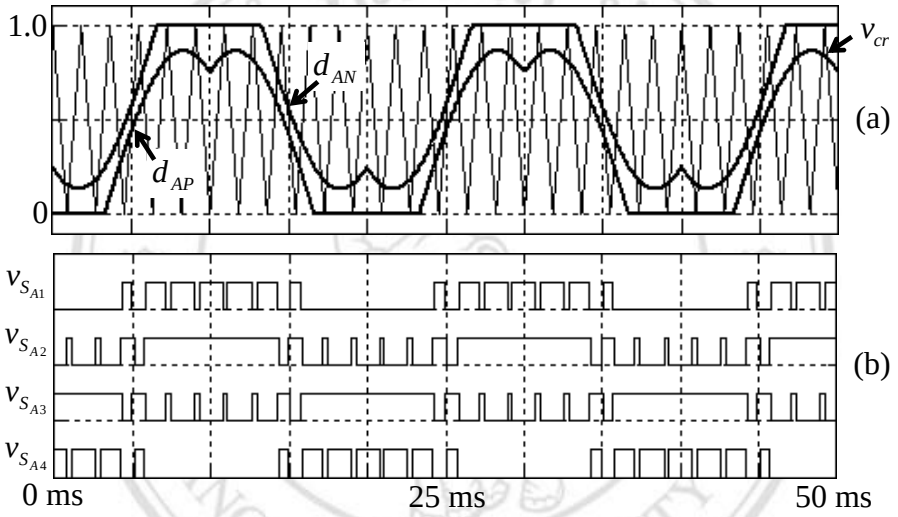


Figure 3.7 Simulation waveforms for leg A (a) the modified duty cycles d_{AP} and d_{AN} (b) gating pulses $v_{S_{A1}} - v_{S_{A4}}$.

Figure 3.7 shows the proposed CB-PWM strategy for the application of a three-level NPC VSI. Figure 3.7 (a) shows the simulated waveforms in leg A with modified duty cycles under the condition of the modulation index m_a = 1.0 and the low switching frequency f_s = 550 Hz. In the proposed CB-PWM strategy, only one triangular carrier wave v_{cr} is used to generate the gating pulses $v_{S_{A1}} - v_{S_{A4}}$, for power switches S_{A1} and S_{A4}, which are generated by comparing the modified duty cycle waveforms d_{AP} and d_{AN} with the triangular carrier wave v_{cr}. The logic of gating pulses for power switches is very simple as follows: if $d_{AP} > v_{cr} \Rightarrow S_{A1} = \text{ON}, S_{A3} = \text{OFF}$ and if

$d_{AN} > v_{cr} \Rightarrow S_{A2} = \text{ON},\ S_{A4} = \text{OFF}$. Since the inner gating pulses S_{A3} and S_{A4} operate are complementary with S_{A1} and S_{A2}, respectively.

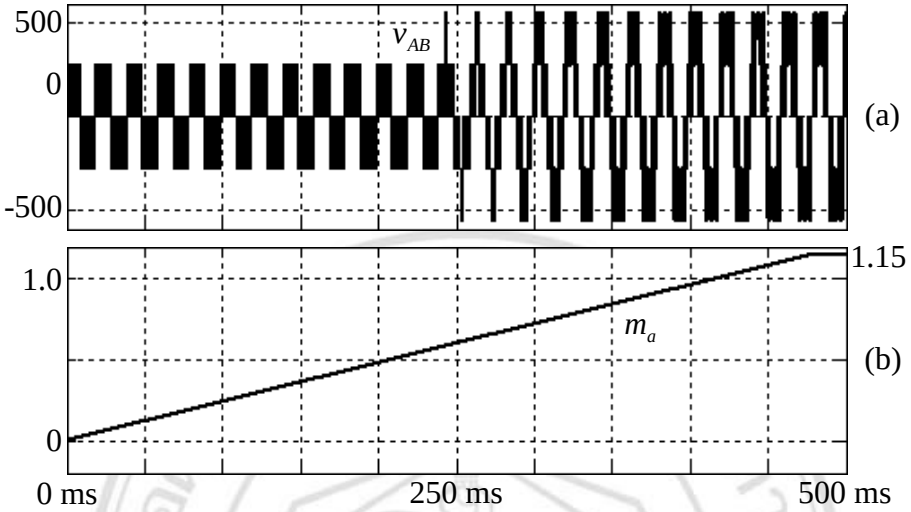


Figure 3.8 Simulation waveforms of dynamic response operation for a ramp modulation index reference (a) line-to-line voltage v_{AB} (b) modulation index m_a.

The proposed CB-PWM strategy, operating in dynamic response, the output voltages of the three-level NPC VSI system are controlled by adjusting the modulation index m_a. Figure 3.8 (a) illustrates the dynamic response for a ramp output line-to-line voltage v_{AB}. The modulation index reference increases starting from zero to maximum value (0 to 1.15) for the linear operation mode in 500 ms, with a switching frequency of 2.5 kHz, as shown in Figure 3.8 (b). As can be seen from the simulated waveform, the line-to-line voltage has five voltage levels at high modulation index and three voltage levels at low modulation index and the result proves that smooth output voltage can be obtained over the whole range of operation.

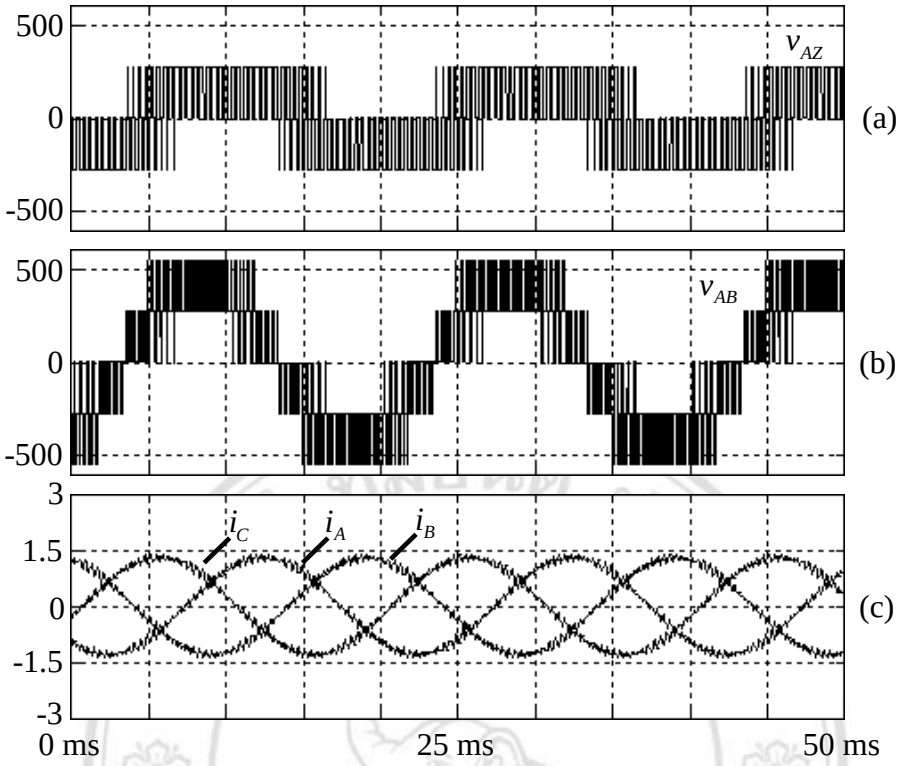


Figure 3.9 Simulation waveforms at high modulation index, m_a = 0.8 (a) pole voltage v_{AZ}, (b) line-to-line voltage v_{AB} (c) phase currents i_A, i_B, i_C.

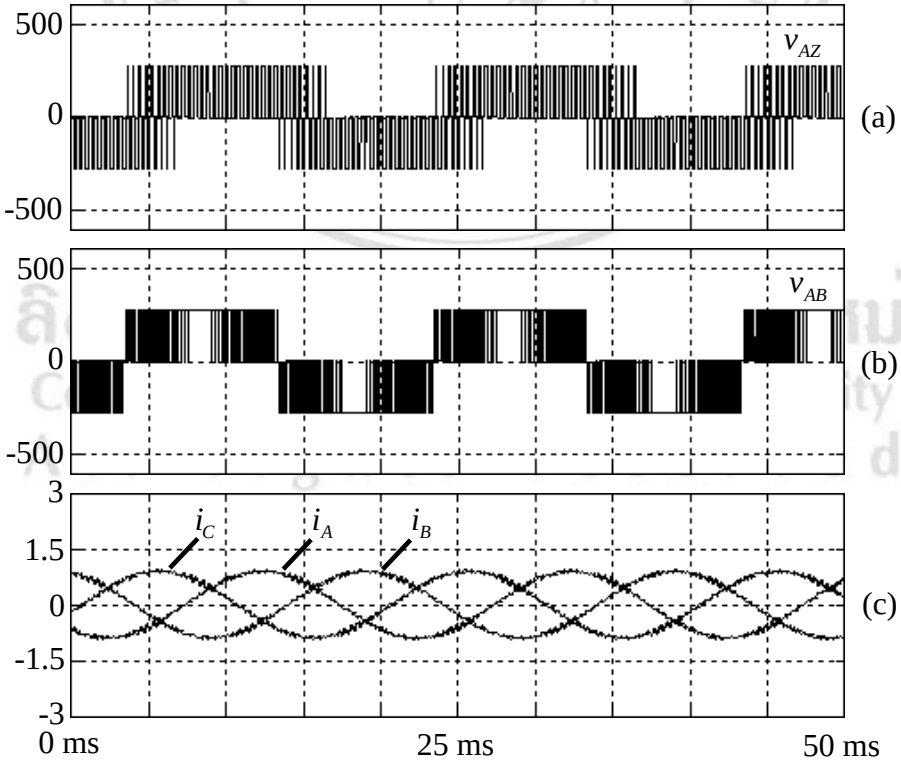


Figure 3.10 Simulation waveforms at low modulation index, m_a = 0.5 (a) pole voltage v_{AZ}, (b) line-to-line voltage v_{AB} (c) phase currents i_A, i_B, i_C.

The output voltage and current waveforms are given in Figure 3.9 and Figure 3.10 with both high (m_a = 0.8) and low modulation (m_a = 0.5) indexes in steady-state conditions. Figure 3.9 shows the simulated output voltage and current waveforms of the three-level NPC VSI in high modulation index, at a switching frequency of 2.5 kHz. The pole voltage, line-to-line voltage and phase currents i_A, i_B, i_C of the inverter are illustrated in Figure 3.9 (a)-(c), respectively. There are three voltage levels on the pole voltage v_{AZ} and the five voltage levels on the line-to-line voltage v_{AB} at high modulation indexes. The simulated waveforms agree with the theoretical analysis. The feasibility of the proposed CB-PWM method and the good quality of the voltage and control signals are verified. It can be seen that the voltages are well balanced in the steady-state operation, while the output phase currents are balanced and almost sinusoidal even when the fundamental frequency switching is under high modulation indexes.

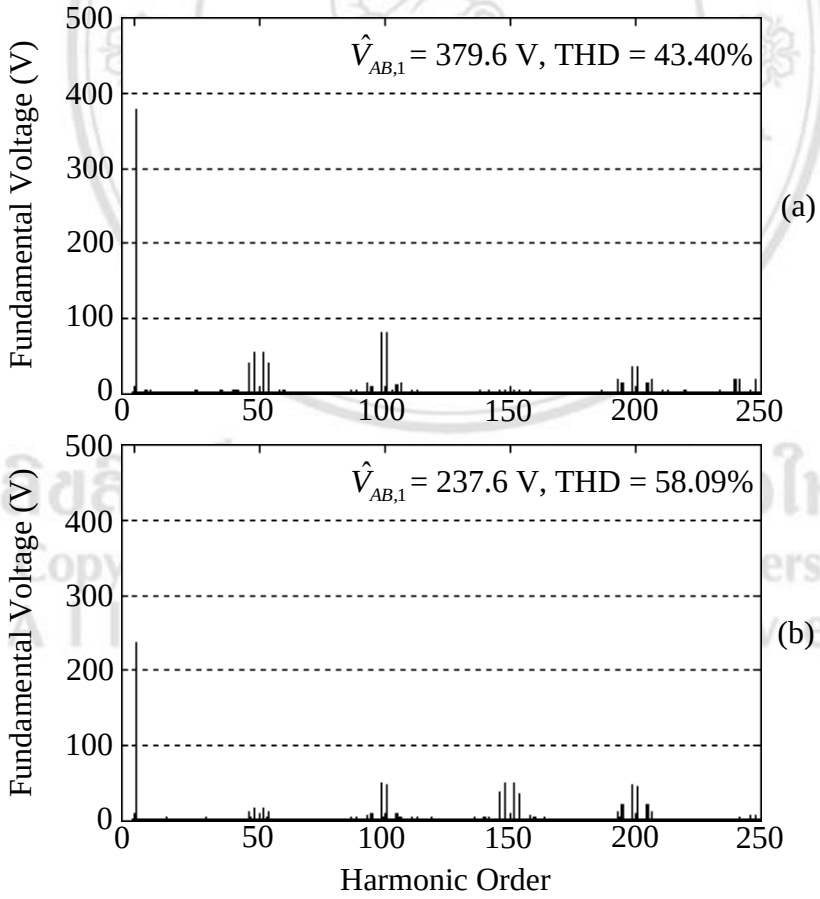


Figure 3.11 Simulation harmonic spectrum of line-to-line voltage v_{AB} with proposed CB-PWM strategy (a) m_a = 0.8 (b) m_a = 0.5.

As the low modulation index, the output voltages and currents of the three-level NPC VSI are illustrated in Figure 3.9. Three voltage levels are generated on the output pole voltage v_{AZ}, and three voltage levels are achieved on the line-to-line voltage v_{AB}, as shown in Figure 3.10 (a) and (b), respectively. In Figure 3.10 (c), the phase currents shown are high quality sinusoids and are well balanced despite the open-loop nature of the proposed method algorithm.

The total harmonic distortion (THD) for line-to-line voltages of three-level NPC VSI with both high and low modulation indices are about 43.40% and 58.09%, respectively, as simulated by MATLAB/Simulink. In Figure 3.11 (a) and (b), the output line-to-line voltage harmonics around the switching frequency for the three-level NPC VSI are 379.6 V and 237.6 V at high and low modulation indexes, respectively. As all simulation results, it can be seen that the proposed CB-PWM is good of a three-level NPC VSI and the voltage balance of the dc-link is controlled fairly well in the whole modulation index range of the steady-state operation, even though the proposed CB-PWM method is simple in its structure.

3.5 Experimental results of CB-PWM strategy

The experimental set-up of the proposed CB-PWM strategy for the three-level NPC VSI is represented by the block diagram shown in Figure 3.12. It consists of a dSPACE DS1103 controller board, a 1 kW four-pole induction motor. A prototype induction motor drive with a front-end three-phase diode bridge rectifier and three-level NPC VSI was built in the laboratory. The setup parameters are the same as those used for the simulation. The inverter output is connected to an induction motor using a standard constant open-loop control method. The machine was unloaded, operating at 50 Hz.

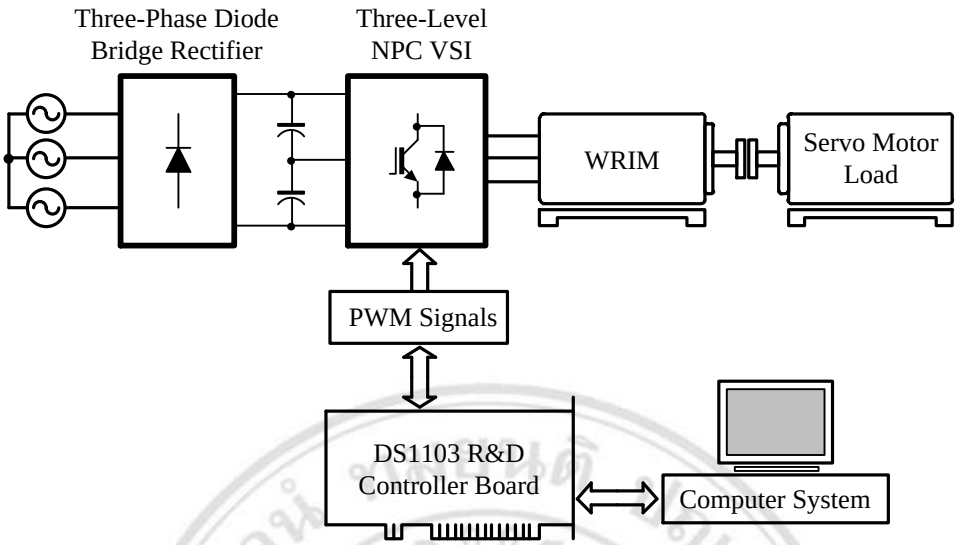
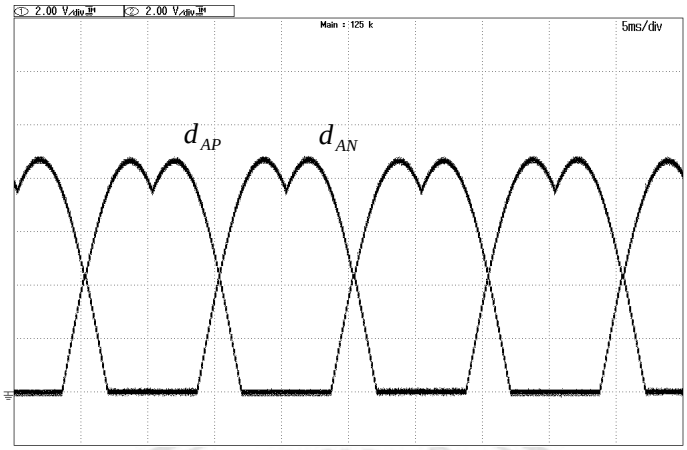
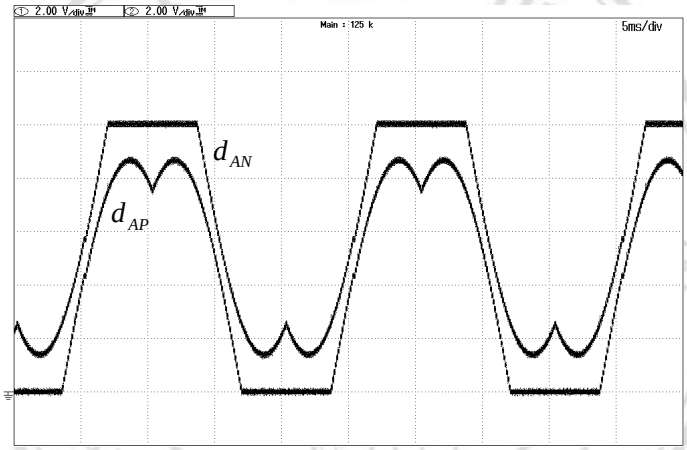


Figure 3.12 Experimental set-up.

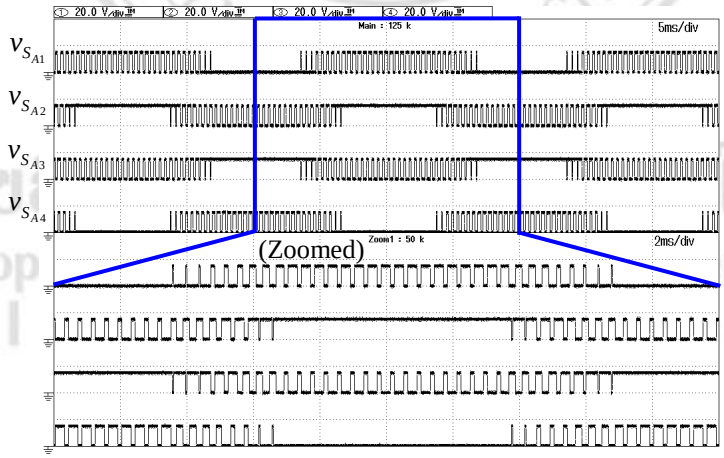
Figure 3.13 shows measured waveforms of duty cycles and gating pulse for power switches. Figure 3.13 (a) shows the duty cycles d_{AP} and d_{AN} of the conventional CB-PWM 2 at the modulation index m_a = 0.8. It can be seen that the upper duty cycles for double signals, which indicate that the duty cycle d_{AP} is the same as d_{AN} but the phase is shifted by π radian. This conventional method requires two triangular carriers to generate the gating pulses. Figure 3.13 (b) shows the proposed modified duty cycles d_{AP} and d_{AN} for leg A at the modulation index m_a = 0.8, which use only one of triangular carrier wave for generate the gating pulses. It can be seen that the experiments resemble the simulation results. The gating pulses of the power switches for leg A in the three-level NPC VSI can be represented in Figure 3.13 (c), which is generated by the proposed CB-PWM strategy. It shows an example of gating pulse arrangements, where $v_{S_{A1}}$ to $v_{S_{A4}}$ are the gating pulses for power switches S_{A1} to S_{A4}, respectively.



(a)



(b)



(c)

Figure 3.13 Experiment waveforms for leg A: (a) the conventional CB-PWM 2 duty cycles d_{AP} and d_{AN} (Scale: 2 V/div), (b) the proposed modified CB-PWM duty cycles d_{AP} and d_{AN} (Scale: 2 V/div), and (c) the proposed modified CB-PWM gating pulses for power switches $v_{S_{A1}}, v_{S_{A2}}, v_{S_{A3}}$, and $v_{S_{A4}}$ (Scale: 20 V/div).

Figure 3.14 shows the experimental waveforms of the dynamic response operation for a ramp modulation index reference, which increases from zero to the maximum modulation index (m_a = 1.15). It can be seen that the output line-to-line voltage waveform proves that smooth output voltage for the linear operation. Therefore, the low modulation index becomes limited to a value which is equal to 0.57.

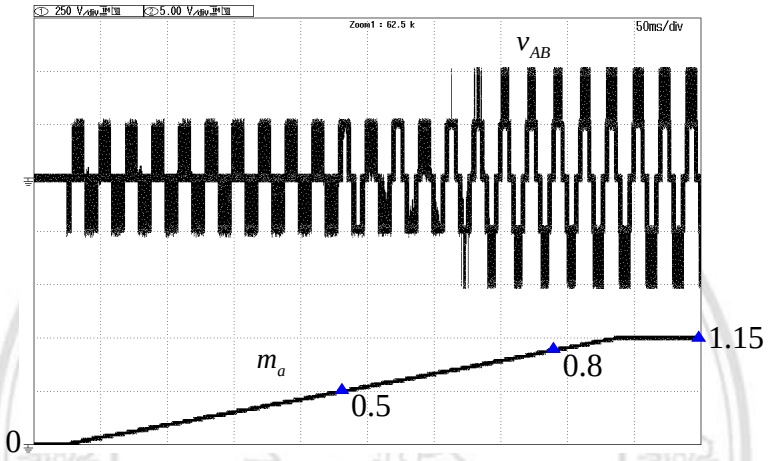
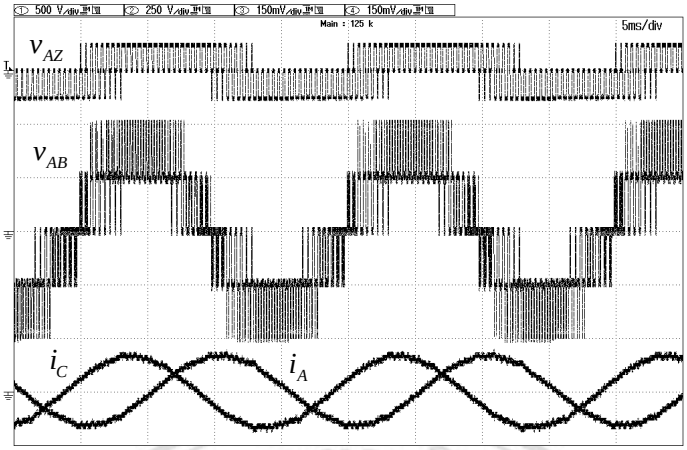
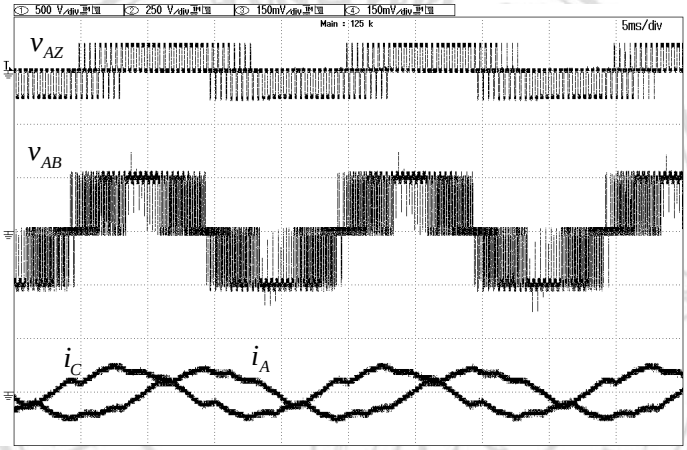


Figure 3.14 Experimental waveforms of dynamic response operation for a ramp modulation index reference: the line-to-line voltage v_{AB} (Scale: 250 V/div) and the modulation index m_a (Scale: 5 V/div).

The inverter voltage and current waveforms in steady-state are shown in Figure 3.15 for high and low modulation indices. It can be seen that from both figures there is good agreement between simulations and experiments, which are obtained in the conditions of Figure 3.9 and Figure 3.10. Figure 3.15 (a) shows the steady-state waveforms of the pole voltage v_{AZ}, line-to-line voltage v_{AB}, and output phase currents i_A, i_C when the inverter operates at the modulation index m_a = 0.8. The line-to-line voltage of the inverter under steady-state operation generated by the five-level inverter can be clearly appreciated in the voltage waveform.



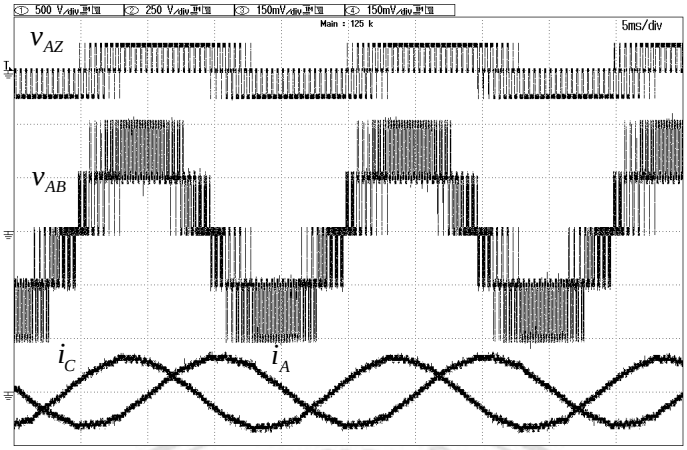
(a)



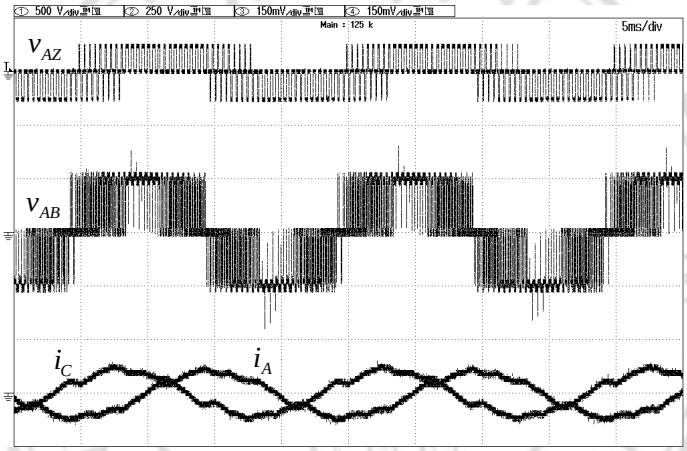
(b)

Figure 3.15 Experiment waveforms of the proposed modified CB-PWM: pole voltage v_{AZ} (Scale: 500 V/div), line-to-line voltage v_{AB} (Scale: 250 V/div), and output phase currents i_A, i_C at no load (Scale: 1.5 A/div) (a) modulation index m_a = 0.8 (b) modulation index m_a = 0.5.

Similarly, Figure 3.15 (b) also shows voltage and current waveforms of the proposed method when applied for low modulation index, m_a = 0.5. From these results, it can be shown that the line-to-line voltage v_{AB} of the inverter under steady-state operation is generated by the three-level voltage and has the amplitude of $V_d / 2$. The line-to-line voltage is identical to that of a conventional two-level inverter. The closely match of simulation and experimental results verifies the feasibility and validity of the proposed strategy. In addition, from both simulation and experimental results, it can be seen that the voltage waveforms generated by the proposed CB-PWM strategy are stable in the steady-state condition.



(a)



(b)

Figure 3.16 Experiment waveforms of the conventional CB-PWM 2: pole voltage v_{AZ} (Scale: 500 V/div), line-to-line voltage v_{AB} (Scale: 250 V/div), and output phase currents i_A, i_C at no load (Scale: 1.5 A/div) (a) modulation index m_a = 0.8 (b) modulation index m_a = 0.5.

Figure 3.16 shows the steady-state voltage and current waveforms of the conventional CB-PWM 2 for high and low modulation indices. It can be seen from both figures that there is good agreement and the experimental results of the proposed method in Figure 3.15 are close to conventional CB-PWM 2. Again, the conventional method requires two triangular carriers for generating the gating pulses, which is a complex implementation**.**

Figure 3.17 shows the harmonic spectrum of the line-to-line voltages of three-level NPC VSI using the proposed CB-PWM strategy with a switching frequency f_s = 2.5 kHz. The fundamental output line-to-line voltage under the condition of m_a = 0.8 and 0.5 had a value of 384.5 V and 238.9 V, respectively. The THD was showed from 46.13% in the high modulation index and 58.88% in the low modulation index. Experimental results and simulated ones presented in Figure 3.17 and Figure 3.11 are in close agreement. Furthermore, in order to verify the performance of the proposed CB-PWM strategy, the simulation results and the experimental results are compared and shown in Table 3.2. It can be observed that the differences of the output voltage and THD for line-to-line voltages between simulation and experimental results are in good agreement for the whole modulation index ranges (0.1-1.15) as shown in Figure 3.18.

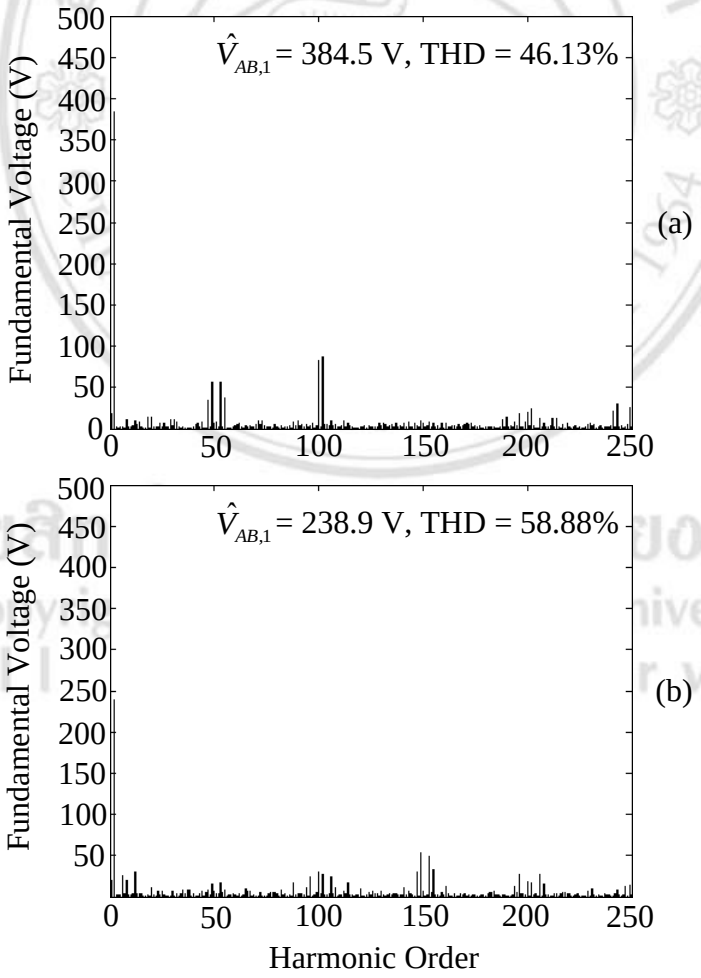


Figure 3.17 Experimental harmonic spectrum of line-to-line voltage with the proposed CB-PWM strategy (a) m_a = 0.8 (b) m_a = 0.5.

Table 3.2 The output voltage and THD for line-to-line voltages between simulation and experimental results under various modulation index.

Modulation index	Simulation results		Experimental results	
	$\hat{V}_{AB,1}$	%THD	$\hat{V}_{AB,1}$	%THD
1.15	545.40	45.89	551.35	47.21
1.1	540.51	46.38	544.63	47.22
1.0	518.45	47.42	520.22	48.53
0.9	428.70	47.64	433.40	48.21
0.8	379.60	44.40	384.50	46.13
0.7	335.30	40.66	336.33	41.39
0.6	292.80	41.11	298.43	42.21
0.5	237.60	58.09	238.90	58.88
0.4	186.60	88.03	191.55	89.05
0.3	144.50	121.74	148.89	123.35
0.2	98.45	158.89	108.95	160.64
0.1	42.15	209.56	49.92	210.62

Figure 3.18 shows the comparison results of the line-to-line voltage total harmonic distortion for the conventional and the proposed CB-PWM strategies. The THD is evaluated for the whole linear modulation index ranges (0.1-1.15) with incremental step size of 0.1 under 2.5 kHz switching frequency condition. It can be seen that the experimental results of the proposed method are close to the conventional CB-PWM strategies (CB-PWM 1 and CB-PWM 2). In all experiments, the output line-to-line voltages THD between the proposed and other conventional CB-PWM strategies are almost no different. However, the proposed method can be implemented easier than other conventional strategies because it uses only one triangular carrier wave for generating the gating pulses in the three-level NPC VSI.

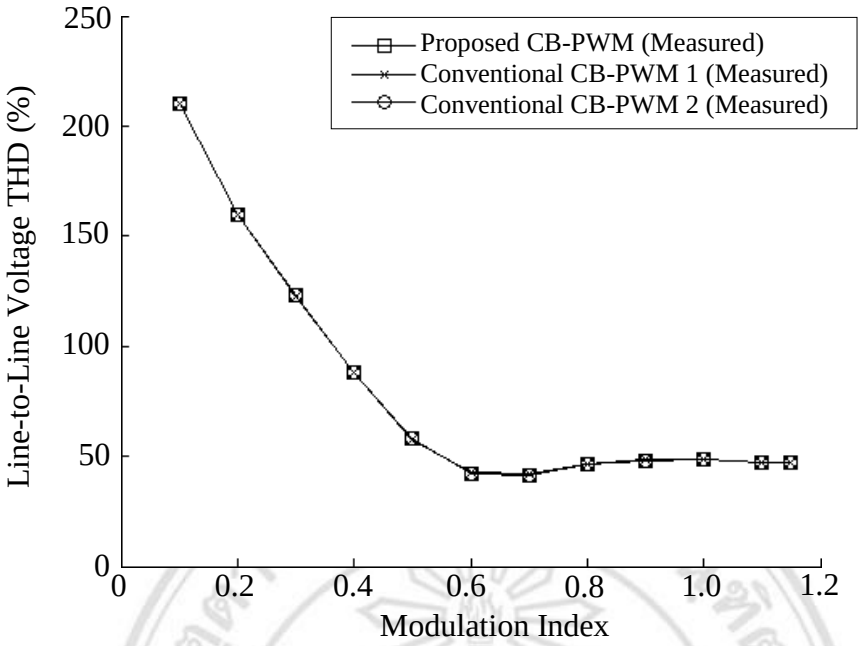


Figure 3.18 THD of the output line-to-line voltages with modulation index of the three-level NPC VSI for different CB-PWM strategies.

3.6 Experimental results of grid-side three-level NPC VSC

An experiment of the grid-connected three-level NPC VSC has been developed to evaluate the proposed CB-PWM strategy which the principle and control system of the grid-side converter controller have been shown in Chapter 5. The performance of the grid-connected three-level NPC VSC based on decoupled vector controller is experimented. The nominal converter dc-link reference voltage is controlled at 180 V, the switching frequency of the converter is 2.5 kHz, and the grid-side converter is connected to the 380V, 50Hz.

3.6.1 Bidirectional power flow with unity power factor operation

The experimental results here show the steady state performance of the grid-side converter at unity power factor operation. Figure 3.19 shows the dc-link voltage v_{dc}, the grid phase voltage v_{ga} and current i_{ga}, and the line-to-line voltage of the grid-side converter v_{iab} operation at unity power factor, the grid reactive power reference Q_g^* is set to zero by the grid-converter for operation in the inverting mode. In this condition, the active power flows from the dc-link into the utility grid. The phase displacement between the

grid phase voltage and the phase current of grid-side converter is out of phase. Similarly, Figure 3.20 also shows the dc-link voltage v_{dc}, the grid phase voltage v_{ga} and current i_{ga}, and the line-to-line voltage of the grid-side converter v_{iab} waveforms in the rectifying mode. In this operation mode, the active power flows into the dc-link, corresponding to sub-synchronous operation of the generator, with in phase displacement between the grid-connected phase voltage and the phase current.

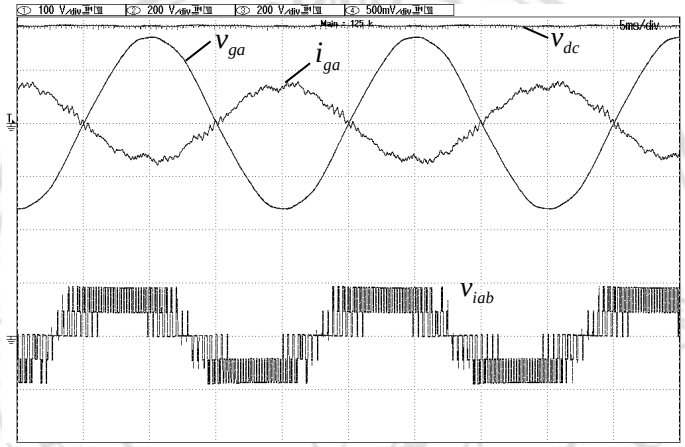


Figure 3.19 Experiment waveforms of the grid-side converter in the inverting mode at unity power factor operation.

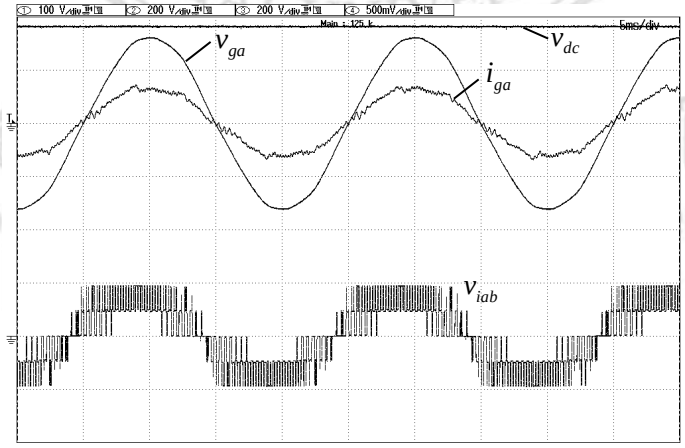


Figure 3.20 Experiment waveforms of the grid-side converter in the rectifying mode at unity power factor operation.

3.6.2 Reactive power flow with lagging and leading power factor operation

The reactive power of the grid-connected three-level NPC VSC can be controlled by adjusting the reference of the reactive power of the utility grid Q_g^*. As can be seen from Figure 3.21, the dynamic response of the grid-side converter in the inverting mode to a step change in reactive power reference control with active power flowing from the dc-link into the utility grid, inverting mode. The setting of reactive power reference is stepped from -120 VAR to +120 VAR and the active power is constant at -400 W. It can be seen that the phase current of grid-side converter can operate under the leading and lagging power factor condition with the performance of the dc-link voltage constant at 180 V. Figure 3.22, the dynamic response of the grid-side converter in the rectifying mode to a step changed in reactive power reference control with active power flowing from the utility grid into the dc-link, rectifying mode. The setting of reactive power reference is stepped from -120 VAR to +120 VAR and the active power is constant at 400 W. It can be seen that the phase current of grid-side converter can operate under the leading and lagging power factor condition, which demonstrates the capability of the grid-side converter to deliver and receive reactive power to the utility grid.

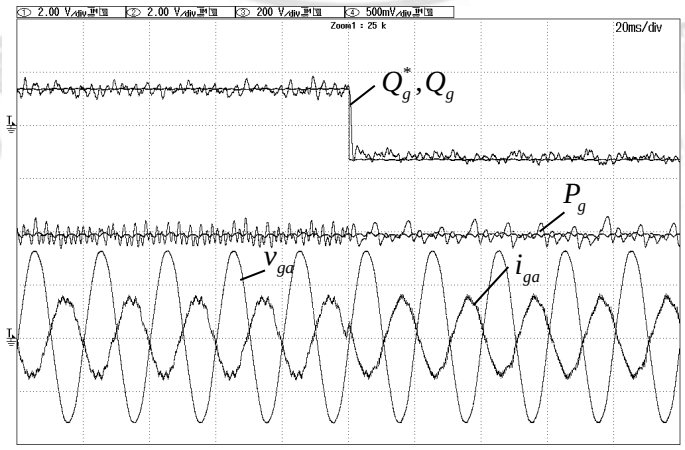


Figure 3.21 Experiment waveforms of dynamic response operation in the inverting mode.

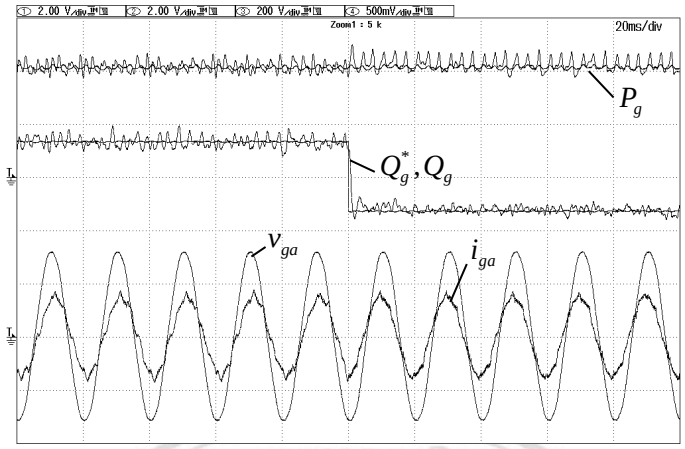


Figure 3.22 Experiment waveforms of dynamic response operation in the rectifying mode.

3.7 Conclusion

This chapter has presented the novel CB-PWM strategy for the three-level NPC VSI. The novelty of the proposed CB-PWM strategy is that only single triangular carrier wave is employed for generating the gating pulses in the three-level NPC VSI and significantly simplifies the modulation strategy. Experimental results confirmed the good performance with quality to the output voltages and the almost sinusoidal output phase currents in the dynamic and steady-state operations under high and low modulation indices. The feasibility and reliability of the proposed modulation strategy have been verified by both computer simulation and experimental results on an induction motor drive system. The main advantages associated are simple PWM algorithm, reduced capacitor voltage ripple, lower switching frequencies, and easy hardware implementation. Finally, this chapter has also proposed the control strategy of vector control for the grid-connected three-level NPC VSC. The objective of the grid-side converter control is to maintain the dc-link voltage and independently active and reactive power flow control. The performance experimental results show that this strategy is able to provide achieve good dynamic responses and high accuracy to the active and reactive power control.