Appendix A Microcontoller use in this research

MICROCHIP

dsPIC30F6010A/6015

dsPIC30F6010A/6015 Enhanced Flash 16-bit Digital Signal Controller (DSC)

Note: This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the "*dsPIC30F Family Reference Manual*" (DS70046). For more information on the device instruction set and programming, refer to the "*dsPIC30F/33F Programmers Reference Manual*" (DS70157).

High-Performance Modified RISC CPU:

- Modified Harvard architecture
- C compiler optimized instruction set architecture with flexible Addressing modes
- 83 base instructions
- 24-bit wide instructions, 16-bit wide data path
- 144 Kbytes on-chip Flash program space (Instruction words)
- 8 Kbytes of on-chip data RAM
- 4 Kbytes of nonvolatile data EEPROM
- Up to 30 MIPS operation:
  - DC to 40 MHz external clock input
  - 4 MHz-10 MHz oscillator input with PLL active (4x, 8x, 16x)
  - 7.37 MHz internal RC with PLL active (4x, 8x, 16x)
- 44 interrupt sources:
  - 5 external interrupt sources
  - 8 user selectable priority levels for each interrupt source
  - 4 processor trap sources
- 16 x 16-bit working register array

DSP Engine Features:

- Dual data fetch
- Accumulator write-back for DSP operations
- Modulo and Bit-Reversed Addressing modes
- Two, 40-bit wide accumulators with optional saturation logic
- 17-bit x 17-bit single-cycle hardware fractional/ integer multiplier
- All DSP instructions single cycle
- ±16-bit single-cycle shift

Peripheral Features:

- High-current sink/source I/O pins: 25 mA/25 mA
- Timer module with programmable prescaler:
  - Five 16-bit timers/counters; optionally pair 16-bit timers into 32-bit timer modules
- 16-bit Capture input functions
- 16-bit Compare/PWM output functions
- 3-wire SPI modules (supports 4 Frame modes)
- I^2C™ module supports Multi-Master/Slave mode and 7-bit/10-bit addressing
- 2 UART modules with FIFO Buffers
- 2 CAN modules, 2.0B compliant (dsPIC306010A)
- 1 CAN module, 2.0B compliant (dsPIC306015)

Motor Control PWM Module Features:

- 8 PWM output channels:
  - Complementary or Independent Output modes
  - Edge and Center-Aligned modes
- 4 duty cycle generators
- Dedicated time base
- Programmable output polarity
- Dead-Time control for Complementary mode
- Manual output control
- Trigger for A/D conversions

Quadrature Encoder Interface Module Features:

- Phase A, Phase B and Index Pulse input
- 16-bit up/down position counter
- Count direction status
- Position Measurement (x2 and x4) mode
- Programmable digital noise filters on inputs
- Alternate 16-bit Timer/Counter mode
- Interrupt on position counter rollover/underflow

dsPIC30F6010A/6015

Analog Features:

- 10-bit Analog-to-Digital Converter (ADC) with 4 S/H Inputs:
  - 1 Msps conversion rate
  - 16 input channels
  - Conversion available during Sleep and Idle
- Programmable Brown-out Reset

Special Microcontroller Features:

- Enhanced Flash program memory:
  - 10,000 erase/write cycle (min.) for industrial temperature range, 100K (typical)
- Data EEPROM memory:
  - 100,000 erase/write cycle (min.) for industrial temperature range, 1M (typical)
- Self-reprogrammable under software control
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Flexible Watchdog Timer (WDT) with on-chip, low-power RC oscillator for reliable operation
- Fail-Safe Clock Monitor operation detects clock failure and switches to on-chip, low-power RC oscillator
- Programmable code protection
- In-Circuit Serial Programming™ (ICSP™)
- Selectable Power Management modes
  - Sleep, Idle and Alternate Clock modes

CMOS Technology:

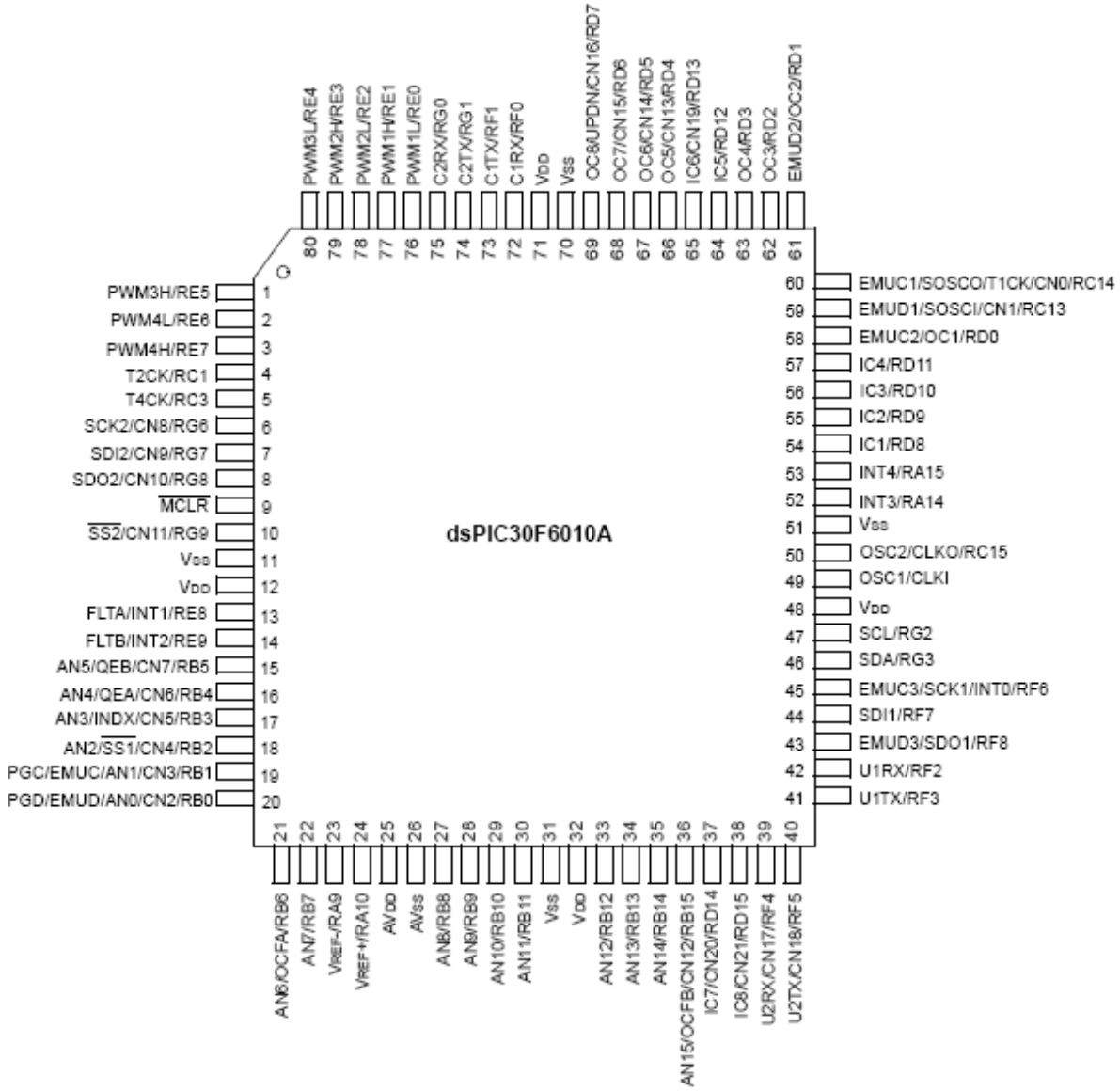
- Low-power, high-speed Flash technology
- Wide operating voltage range (2.5V to 5.5V)
- Industrial and Extended temperature ranges
- Low-power consumption

dsPIC30F Motor Control and Power Conversion Family*

Device	Pins	Program Mem. Bytes/ Instructions	SRAM Bytes	EEPROM Bytes	Timer 16-bit	Input Cap	Output Comp/Std PWM	Motor Control PWM	A/D 10-bit 1 Msps	Quad Enc	UART	SPI	I²C™	CAN
dsPIC30F2010	28	12K/4K	512	1024	3	4	2	6 ch	6 ch	Yes	1	1	1	—
dsPIC30F3010	28	24K/8K	1024	1024	5	4	2	6 ch	6 ch	Yes	1	1	1	—
dsPIC30F4012	28	48K/16K	2048	1024	5	4	2	6 ch	6 ch	Yes	1	1	1	1
dsPIC30F3011	40/ 44	24K/8K	1024	1024	5	4	4	6 ch	9 ch	Yes	2	1	1	—
dsPIC30F4011	40/ 44	48K/16K	2048	1024	5	4	4	6 ch	9 ch	Yes	2	1	1	1
dsPIC30F5015	64	66K/22K	2048	1024	5	4	4	8 ch	16 ch	Yes	1	2	1	1
dsPIC30F5016	80	66K/22K	2048	1024	5	4	4	8 ch	16 ch	Yes	1	2	1	1
dsPIC30F6010A	80	144K/48K	8192	4096	5	8	8	8 ch	16 ch	Yes	2	2	1	2
dsPIC30F6015	64	144K/48K	8192	4096	5	8	8	8 ch	16 ch	Yes	2	2	1	1

* This table provides a summary of the dsPIC30F peripheral features. Other available devices in the dsPIC30F Motor Control and Power Conversion Family are shown for feature comparison.

80-Pin TQFP



Appendix B VSG Schematics diagram and PCB designed

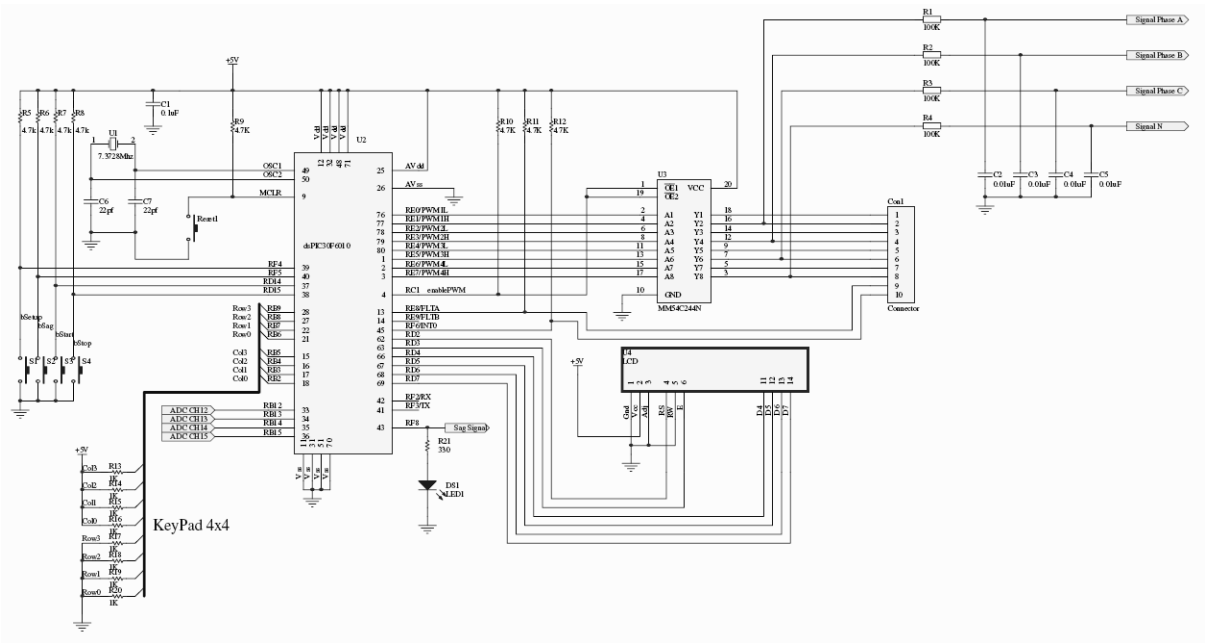


Figure AB-1 A Microcontroller dsPIC30F6010a controller schematic diagram

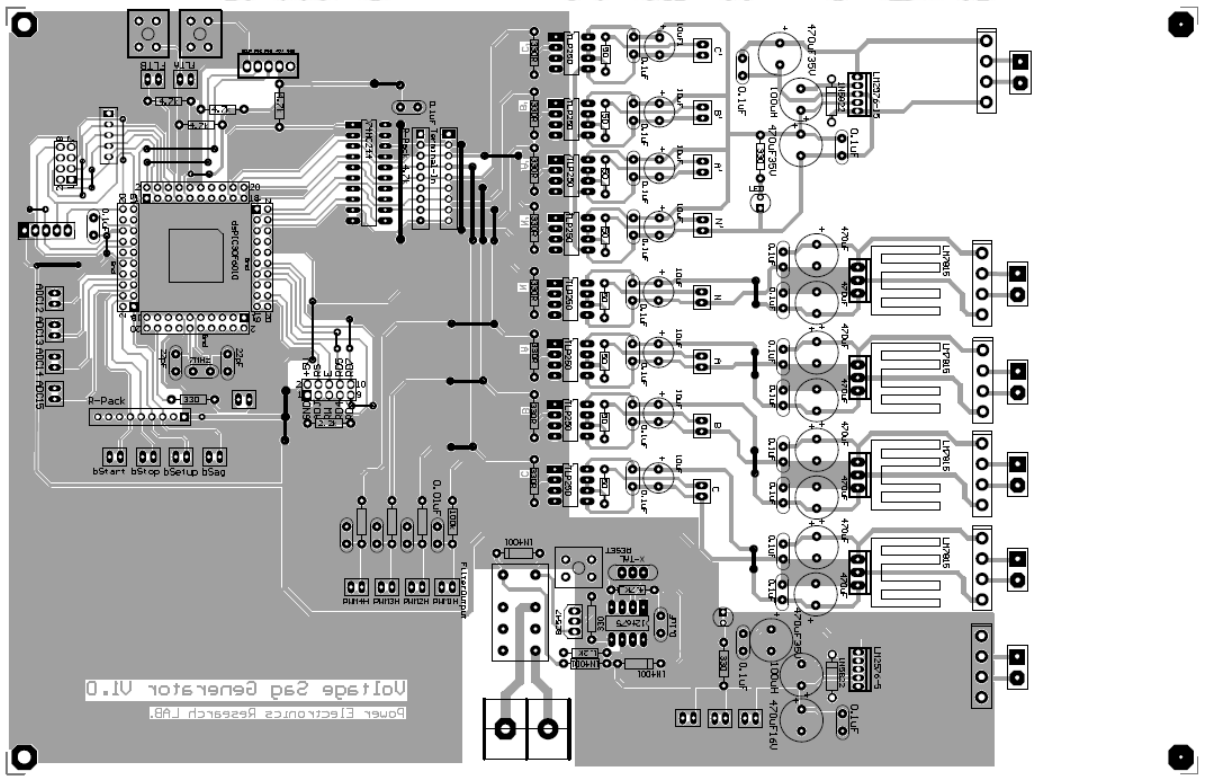


Figure AB-2 A Microcontroller dsPIC30F6010a controller PCB

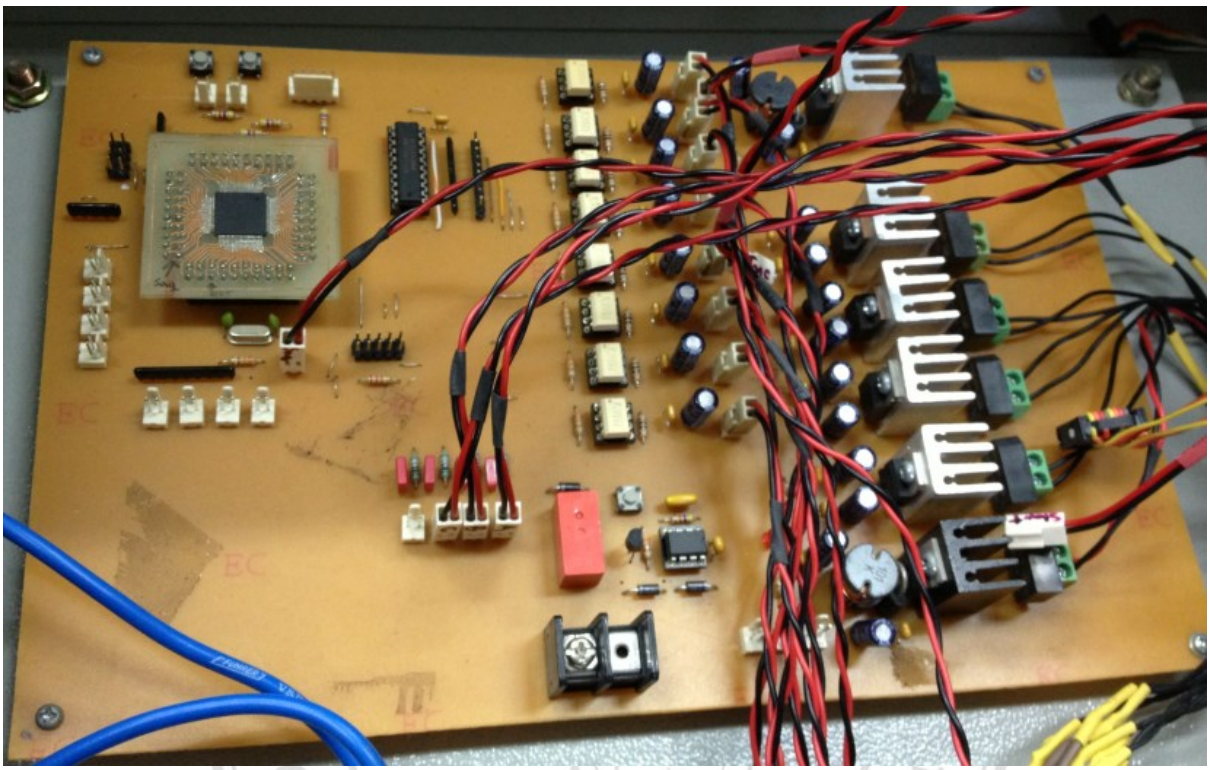


Figure AB-3 A Microcontroller dsPIC30F6010a controller PCB

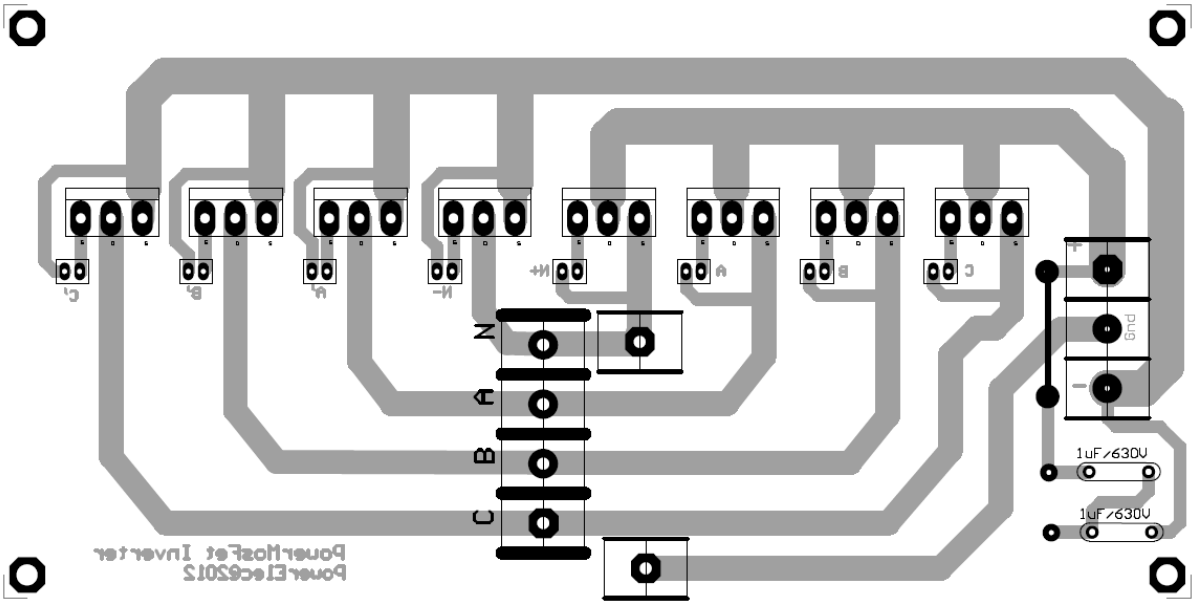


Figure AB-4 IGBT power part PCB

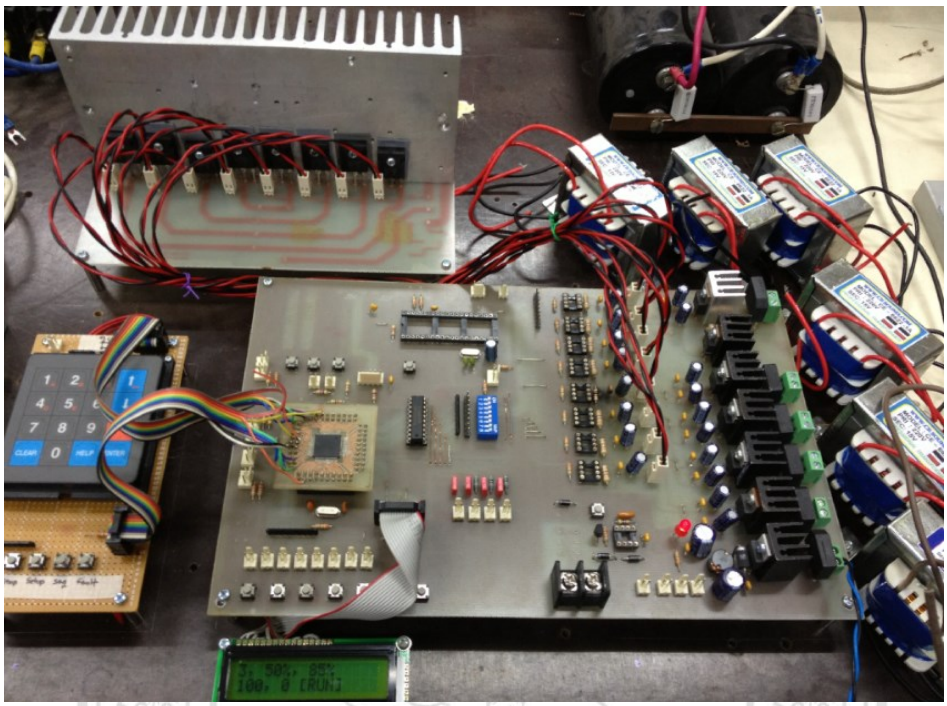


Figure AB-5 Overall system of VSG

Figure ABS-6 Overall system of VSG testing EUT

CURRICULUM VITAE

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W. Muangjai, S. Premrudeepreechacharn, K. Oranpiroj, W. Jantee, "A Three-Phase Four-Leg Voltage Sag Generator with Carrier-Based PWM Technique for Testing Electrical Equipment", Pullman Bangkok King Power, Bangkok, Thailand, 30-31 May 2013