CHAPTER 3

Designed voltage sags generator with carrier-based PWM technique

In this chapter purposed modulation method for 3-phase 4-wire converter using Carrier-Based PWM technique. And design voltage sags algorithm with c programing language using dsPIC microcontroller for control VSG and finally designed LC Low-pass filter for improve THDv and THDi AC voltage and current output. Before design this research using PSIM program and MATLAB GUI run simulation to improve hypothesis.

3.1 Structure of voltage sags generator

Figure 3.1 shows the main components can be used in order to model the VSG. In all models used in simulations, following four main parts of the VSG can be distinguished

1) The DC voltage supply system
2) The DC/AC voltage inverter (with IGBT driver circuit)
3) The output LC filter
4) The microcontroller and parts

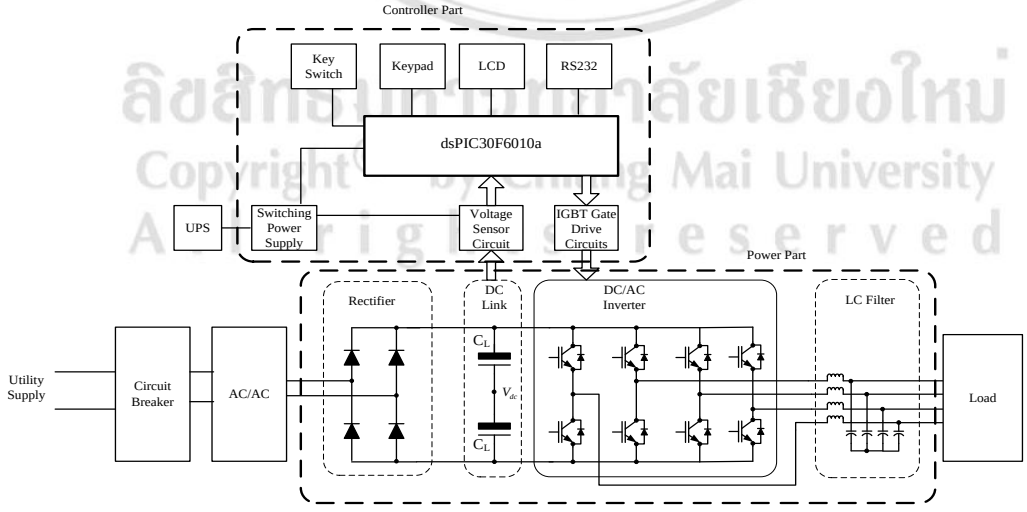


Figure 3.1 Main component of VSG

3.2 The 3-phase 4-wire voltage source inverter topology

The 3-phase 4-wire voltage source inverter topology has advantage than other topology shows in table 1.1 and provides a 3 phase output with neutral connection. The topology of this hardware consists of AC/DC power converter and a 4 leg IGBT inverter. The configuration of a 3-phase 4-wire voltage sag compensator is shown as a block diagram in Figure 3.2

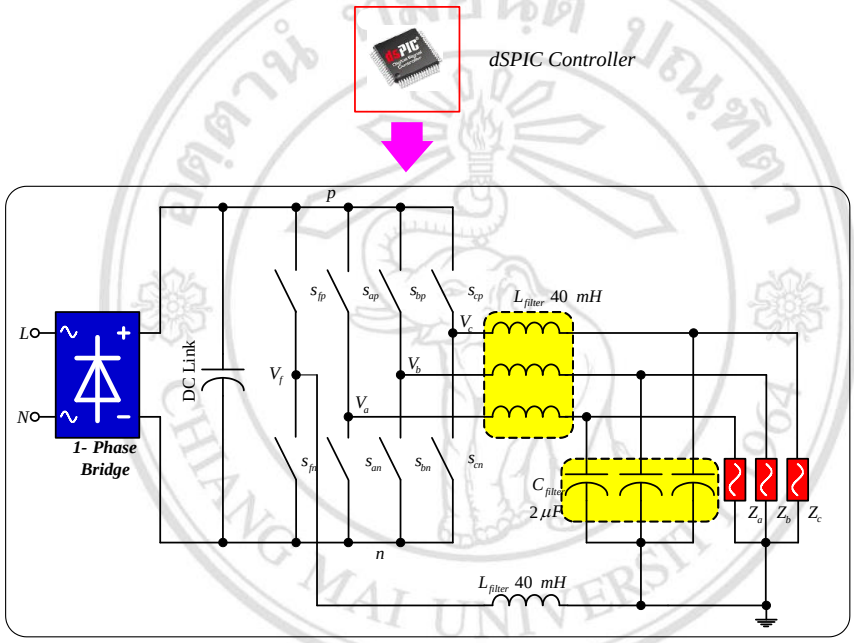


Figure 3.2 Three-phase four-leg voltage source converter topology considered in this thesis.

The operation of the 3-phase 4-wire voltage source inverter proceeds as follows. The full wave rectifier converts the AC output supply from transformer 220VAC to 500VAC rectifier to DC voltage about 700VDC with bridge rectifier. The constant DC link voltage is converted by the DC/AC inverter (3-phase 4-leg inverter) to AC voltage 3 phase 4 wire using carrier-based pulse width modulation technique CBPWM, detailed in the following section. This condition is maintained during the entire duration of the voltage sag.

3.3 Carrier-based PWM (CBPWM) technique for 3-phase 4-wire voltage source inverter

A 3-phase 4-wire voltage source inverter topology, as shown in Figure 3.2. And [23], [24] was presented a carrier-based PWM (CBPWM) technique for three-phase four-leg inverter, an improved the 3D SVPWM algorithm achieves results that are comparable with CBPWM with technique increase the utilization of DC link voltage 15% than sine PWM [27]. Therefore, in this research purpose a voltage sags generator using CBPWM technique and implement software algorithm to dsPIC microcontroller shown in Figure 3.3

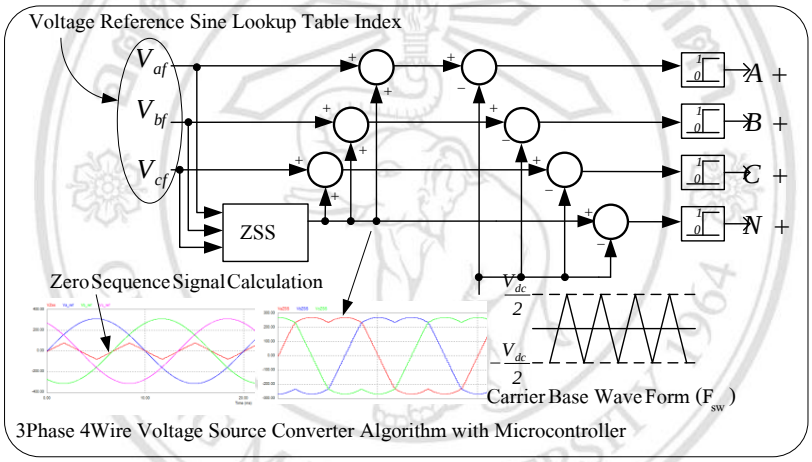


Figure 3.3 A carrier-based PWM technique (CBPWM)

The operation of PWM can be divided into two modes [22], [23] and carrier modulation with PWM shown Figure 3.4

1) Linear Mode.—In the linear mode, the peak of a modulation signal is less than or equal to the peak of the carrier signal. When the carrier frequency /car is greater than 20X modulation signal frequency /, the gain of PWM G $\approx$ 1.

2) Nonlinear Mode—When the peak of a modulation signal is greater than the peak of the carrier signal, overmodulation occurs with G < 1. The six-step mode marks the end of the nonlinear mode. The THD of output switched waveforms increases

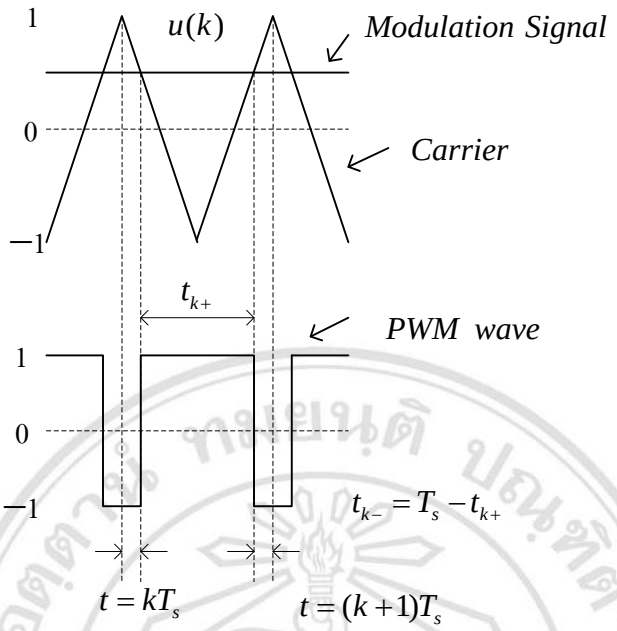


Figure 3.4 Two level carrier-based PWM

In the linear modulation range, neglecting high order harmonics the output line-to-neutral votages V_{pN} $(p = a,b,c)$

$$V_{pN} = \frac{V_{DC}}{2} v_p \qquad (p = a,b,c) \tag{3.1}$$

where *N* is the neutral point of the dc bus.

A universal representation of modulation signals $v_p(t)$ $(p = a,b,c)$ for three-phase carrier PWM modulators is as follows (3.2)

$$v_p(t) = v_p^*(t) + e_i(t) \tag{3.2}$$

where $e_i(t)$ are injected harmonics, and v_p^* are called fundamental signals that are three-phase symmetrical sinusoidal signals as follows:

$$\left.\begin{aligned} v_a^*(t) &= m\sin\omega t \\ v_b^*(t) &= m\sin(\omega t + \frac{2\pi}{3}) \\ v_c^*(t) &= m\sin(\omega t + \frac{4\pi}{3}) \end{aligned}\right\} \tag{3.3}$$

where m is the modulation index, and $v_a^*(t) + v_b^*(t) + v_c^*(t) = 0$. According to (3.1) and (3.3), the output line-to-neutral voltages V_{pN} $(p = a,b,c)$ and $e_i(t)$ are injected

$$\left.\begin{aligned} V_{aN}(t) &= \frac{V_{DC}}{2}[m\sin\omega t + e_i(t)] \\ V_{bN}(t) &= \frac{V_{DC}}{2}[m\sin(\omega t + \frac{2\pi}{3}) + e_i(t)] \\ V_{cN}(t) &= \frac{V_{DC}}{2}[m\sin(\omega t + \frac{4\pi}{3}) + e_i(t)] \end{aligned}\right\} \tag{3.4}$$

The output line-to-line voltages V_{ab}, V_{bc} และ V_{ca} are

$$\left.\begin{aligned} V_{ab}(t) &= V_{aN}(t) - V_{bN}(t) \\ &= \frac{V_{DC}}{2}\sqrt{3}\,m\sin(\omega t + \frac{\pi}{6}) \\ V_{bc}(t) &= \frac{V_{DC}}{2}\sqrt{3}\,m\sin(\omega t + \frac{5\pi}{6}) \\ V_{ca}(t) &= \frac{V_{DC}}{2}\sqrt{3}\,m\sin(\omega t + \frac{3\pi}{2}) \end{aligned}\right\} \tag{3.5}$$

In the linear modulation range, (3.4), (3.5), and $|v_i| \le 1$ show that output line-to-line voltages are equal to or less than dc-bus voltage *E*. Therefore, the possible maximum modulation index $m_{\max x}$ is $2/\sqrt{3}$ in the linear range, and we have

$$-1 - v_{\min}^*(t) \le e_i(t) \le 1 - v_{\max}^*(t) \tag{3.6}$$

Where $v_{\min}^*(t) = \min\{v_a^*(t), v_b^*(t), v_c^*(t)\}$ and $v_{\max}^*(t) = \max\{v_a^*(t), v_b^*(t), v_c^*(t)\}$ It is clear

that the injected harmonics $e_i(t)$ do not appear in the line-to-line voltages. Therefore, $e_i(t)$ is usually called as *zero sequence signal* and $e_i(t)$ can be calculated by

$$e_i(t) = \frac{1}{3}\left[v_a(t) + v_b(t) + v_c(t)\right] \tag{3.7}$$

$e_i(t) = 0$ Yields *sinusoidal* PWM. In the linear range, from (3.3) (3.5) and $|v_i| \le 1$, we have $m_{\max} = 1$ and the maximum output line-to-line voltages are $\sqrt{3}V_{DC}/2$ modulation occurs. When $m > 1$, over modulation occurs.

When $e_i(t) \neq 0$, *nonsinusoidal* PWM occurs. When $e_i(t)$ is a suitable signal, such as $e_i(t) = \frac{m}{6}\sin(\omega t)$, all the tops of $v_i^*(t)$ are cut by $e_i(t)$ $m_{\max} = 2/\sqrt{3}$ and the maximum output line-to-line voltages reach V_{DC} in the linear range.

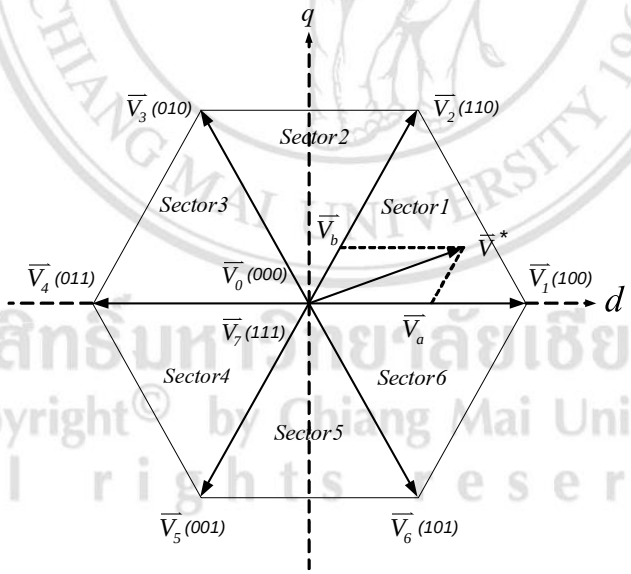
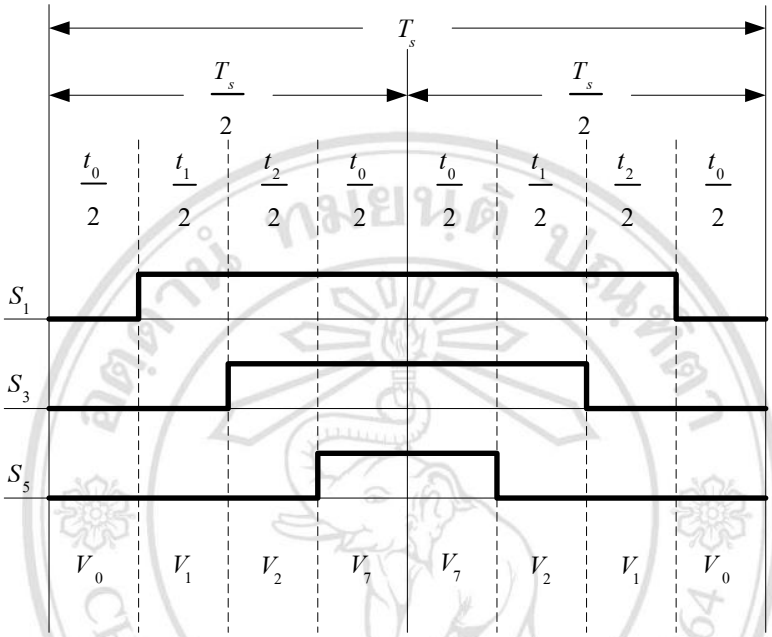


Figure 3.5 Voltage switching vector

3.4 Calculation voltage reference v_{Ao} , v_{Bo} and v_{Co} for zero signal sequence (ZSS)

From the previous example switching stats in Figure 3.5 for calculation $\bar{V}^*$ in sector 1 from Figure 3.5



Figture 3.6 Eight switching states in sector 1

From Figure 3.4 v_{Ao} are

$$v_{Ao} = \frac{\left(t_1 + t_2 + t_7\right)\frac{V_{DC}}{2} + t_0\left(\frac{-V_{DC}}{2}\right)}{T_S} = \frac{t_1 + t_2}{T_S}\frac{V_{DC}}{2} \quad ; t_0 = t_7 \tag{3.7}$$

when $t_1 = t_a, t_2 = t_b$:

$$\begin{aligned} \frac{t_a}{T_s} &= \frac{\sqrt{3}A}{V_{DC}}\sin\left(\frac{\pi}{3} - \theta\right) \\ \frac{t_b}{T_S} &= \frac{\sqrt{3}A}{V_{DC}}\sin\left(\theta\right) \end{aligned} \tag{3.8}$$

$$\left.\begin{aligned}\frac{t_1}{T_S}+\frac{t_2}{T_S} &= \frac{\sqrt{3}A}{V_{DC}}\left(\sin\left(\frac{\pi}{3}-\theta\right)+\sin\theta\right)\\ &= \frac{\sqrt{3}A}{V_{DC}}\left(\sin\frac{\pi}{3}\cos\theta-\cos\frac{\pi}{3}\sin\theta+\sin\theta\right)\\ &= \frac{\sqrt{3}A}{V_{DC}}\left(\frac{\sqrt{3}}{2}\cos\theta+\frac{\sin\theta}{2}\right)\\ &= \frac{\sqrt{3}A}{V_{DC}}\cos\left(\theta-\frac{\pi}{6}\right)\end{aligned}\right\} \quad (3.9)$$

Thus

$$\left.\begin{aligned}v_{Ao} &= \frac{\sqrt{3}A}{V_{DC}}\frac{V_{DC}}{2}\cos\left(\theta-\frac{\pi}{6}\right)\\ &= \frac{\sqrt{3}A}{2}\cos\left(\theta-\frac{\pi}{6}\right)\end{aligned}\right\} \quad (3.10)$$

and

$$v_{Bo} = \frac{\left(t_2+t_7\right)\frac{V_{DC}}{2}+\left(t_0+t_1\right)\left(\frac{-V_{DC}}{2}\right)}{T_S} = \frac{t_2-t_1}{T_S}\frac{V_{DC}}{2} \quad ; t_0 = t_7 \quad (3.11)$$

$$\left.\begin{aligned}\frac{t_a}{T_s} &= \frac{\sqrt{3}A}{V_{DC}}\sin\left(\frac{\pi}{3}-\theta\right)\\ \frac{t_b}{T_S} &= \frac{\sqrt{3}A}{V_{DC}}\sin\left(\theta\right)\end{aligned}\right\} \quad (3.12)$$

$$\left.\begin{aligned}\frac{t_2-t_1}{T_S} &= \frac{\sqrt{3}A}{V_{DC}}\sin(\theta)-\frac{\sqrt{3}A}{V_{DC}}\sin\left(\frac{\pi}{3}-\theta\right)\\ &= \frac{\sqrt{3}A}{V_{DC}}\left(\sin(\theta)-\left(\sin\frac{\pi}{3}\cos\theta-\cos\frac{\pi}{3}\sin\theta\right)\right)\\ &= \frac{\sqrt{3}A}{V_{DC}}\left(\sin(\theta)-\left(\frac{\sqrt{3}}{2}\cos\theta-\frac{1}{2}\sin\theta\right)\right)\\ &= \frac{\sqrt{3}A}{V_{DC}}\left(\frac{3}{2}\sin(\theta)-\frac{\sqrt{3}}{2}\cos\theta\right)\\ &= 3A\left(\frac{\sqrt{3}}{2}\sin\theta-\frac{\cos\theta}{2}\right)\\ &= 3A\cos(\theta-\frac{2\pi}{3})\end{aligned}\right\} \quad (3.13)$$

$$v_{Bo} = \frac{3A}{2}\cos\left(\theta-\frac{2\pi}{3}\right) \quad (3.14)$$

and

$$v_{Co} = \frac{(t_7)\frac{V_{DC}}{2}+(t_0+t_1+t_2)\left(\frac{-V_{DC}}{2}\right)}{T_S} = \frac{-(t_2+t_1)}{T_S}\frac{V_{DC}}{2} \quad ; t_0 = t_7 \quad (3.15)$$

It was similar to the equation (3.8) equal $(-v_{Ao})$

$$v_{Co} = -\frac{\sqrt{3}A}{2}\cos\left(\theta-\frac{\pi}{6}\right) = -v_{Ao} \quad (3.16)$$

To see that now v_{Ao}, v_{Bo} and v_{Co} which can then be compared with triangular signal to be modulated pulse width. This will be a signal to the driver to bring the power inverter, but from equation (3.8), (3.9) and (3.10) is the equation used in sector 1, so find an equation for calculating the voltage reference. Other sectors with by the above methods are difficult to find. And require more time to calculate. Is there a way to find a faster and easier to follow.

from $\quad \bar{V}^* = x + jy, \quad x = A\cos\theta, y = A\sin\theta$

and $\quad v_{An} = \mathrm{Re}\left[\vec{V}^*\right] = A\cos\theta \quad (3.17)$

$$v_{Bn} = \mathrm{Re}\left[a^2 \bar{V}^* \right] = A\cos\left(\theta - \frac{2\pi}{3} \right) \tag{3.18}$$

$$v_{Cn} = \mathrm{Re}\left[a\bar{V}^* \right] = A\cos\left(\theta + \frac{2\pi}{3} \right) \tag{3.19}$$

Considering zero sequence voltage (Zero Sequence Voltage, v_{no}) from sector 1 That is

$$v_{no} = \frac{1}{3}\left(v_{Ao} + v_{Bo} + v_{Co} \right) = \frac{A}{2}\cos\left(\theta - \frac{2\pi}{3} \right) = \frac{1}{2} v_{Bn} \tag{3.20}$$

From equation (3.10), (3.11) and (3.12) v_{Bo} is mean voltage (Median) thus v_{Bn} is the middle value when compared to the v_{An} and v_{Cn}

Considering $\bar{V}^*$ in sector 2 we have $\alpha_1 = \frac{\pi}{3}$, $\alpha_2 = \frac{2\pi}{3}$ and $\frac{\pi}{3} \le \theta \le \frac{2\pi}{3}$ therefore requires a space vector of voltage follow $\vec{V}_2, \vec{V}_3, \vec{V}_0, \vec{V}_7$. Then, using equations (3.18) to calculate the time to switch to.

$$\begin{bmatrix} \frac{t_a}{T_S} \\ \frac{t_b}{T_S} \end{bmatrix} = \frac{\sqrt{3}A}{V_{DC}} \begin{bmatrix} \sin\left(\frac{2\pi}{3} - \theta \right) \\ \sin\left(\theta - \frac{\pi}{3} \right) \end{bmatrix} \tag{3.21}$$

Thus

$$t_2 = t_a ; t_3 = t_b$$
$$T_S = t_2 + t_3 + t_0 + t_7$$
$$t_0 = t_7$$

We can draw a pattern switching in sector 2 in Figure 3.6

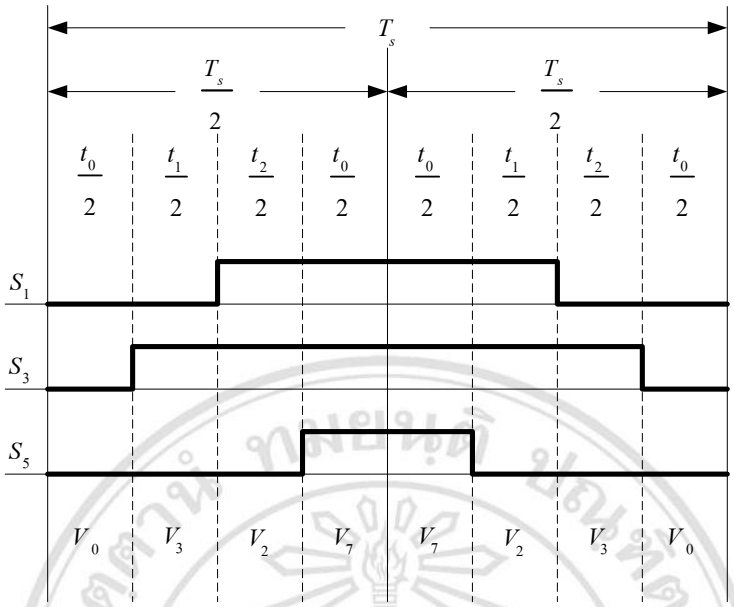


Figure 3.7 Switching Pattern in Sector 2

Calculate v_{Ao}, v_{Bo} and v_{Co} use same formula in sector 1

$$\left.\begin{aligned} v_{Ao} &= \frac{3A}{2}\cos\theta \\ v_{Bo} &= \frac{\sqrt{3}A}{2}\sin\theta \\ v_{Co} &= -\frac{\sqrt{3}A}{2}\sin\theta = -v_{Bo} \end{aligned}\right\} \tag{3.22}$$

Find Zero sequence signal voltage

$$v_{no} = \frac{1}{3}\left(v_{Ao} + v_{Bo} + v_{Co}\right) = \frac{A}{2}\cos\theta = \frac{1}{2}v_{An} \tag{3.23}$$

In sector 2 v_{Ao} is median voltage thus v_{An} is median voltage compare by v_{Bn} and v_{Cn}

Sector 3

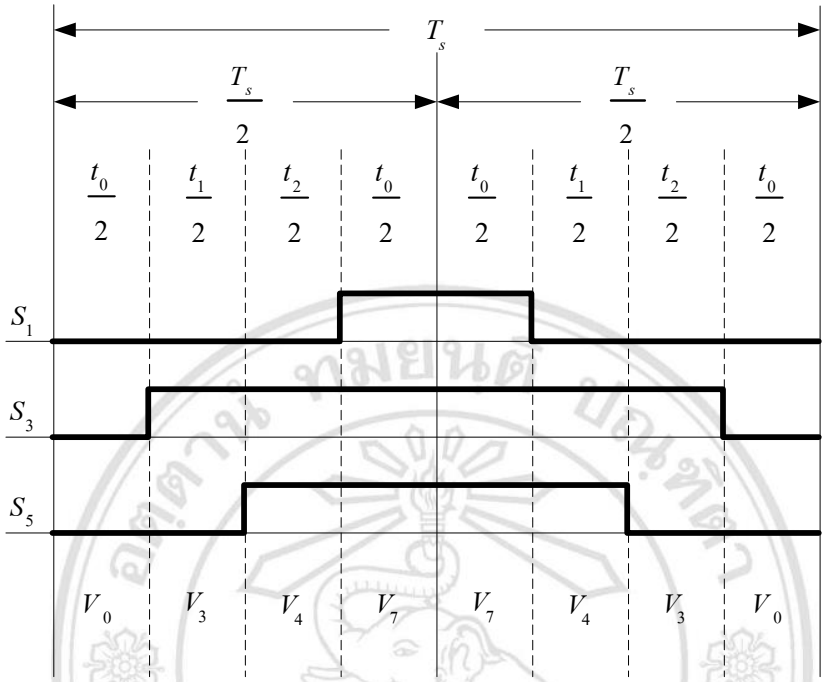


Figure 3.8 Switching pattern in sector 3

Calculate v_{Ao}, v_{Bo} and v_{Co} use same formula in sector 1

$$\left.\begin{aligned} v_{Ao} &= \frac{\sqrt{3}A}{2}\cos\left(\theta+\frac{\pi}{6}\right) \\ v_{Bo} &= -\frac{\sqrt{3}A}{2}\cos\left(\theta+\frac{\pi}{6}\right) = -v_{Ao} \\ v_{Co} &= \frac{3A}{2}\cos\left(\theta+\frac{2\pi}{3}\right) \end{aligned}\right\} \quad (3.24)$$

Find Zero sequence signal voltage

$$v_{no} = \frac{A}{2}\cos\left(\theta+\frac{2\pi}{3}\right) = \frac{1}{2}v_{Cn} \quad (3.25)$$

Sector 4

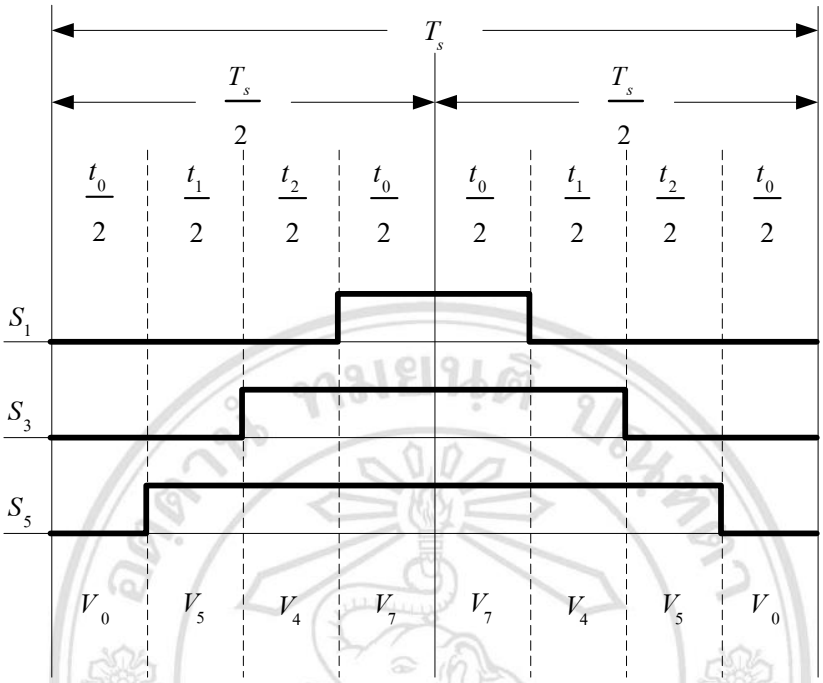


Figure 3.9 Switching pattern in sector 4

Calculate v_{Ao}, v_{Bo} and v_{Co} use same formula in sector 1

$$\left.\begin{aligned} v_{Ao} &= \frac{\sqrt{3}A}{2}\cos\left(\theta-\frac{\pi}{6}\right) \\ v_{Bo} &= \frac{3A}{2}\cos\left(\theta-\frac{2\pi}{3}\right) \\ v_{Co} &= -\frac{\sqrt{3}A}{2}\cos\left(\theta-\frac{\pi}{6}\right) = -v_{Ao} \end{aligned}\right\} \tag{3.26}$$

Find Zero sequence signal voltage

$$v_{no} = \frac{A}{2}\cos\left(\theta-\frac{2\pi}{3}\right) = \frac{1}{2}v_{Bn} \tag{3.27}$$

Sector 5

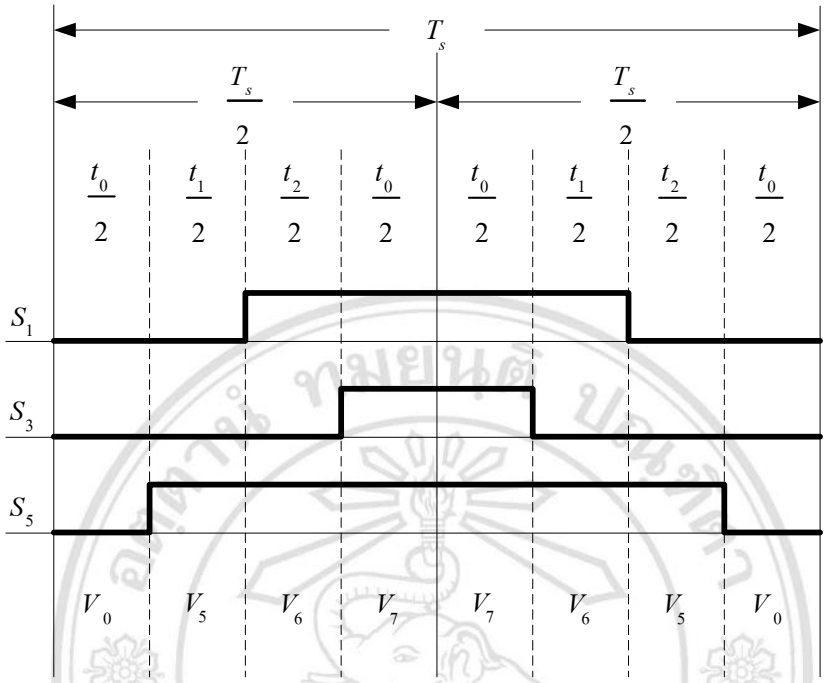


Figure 3.10 Switching pattern in sector 5

Calculate v_{Ao}, v_{Bo} and v_{Co} use same formula in sector 1

$$\left.\begin{aligned} v_{Ao} &= \frac{3A}{2}\cos\theta \\ v_{Bo} &= \frac{\sqrt{3}A}{2}\sin\theta \\ v_{Co} &= -\frac{\sqrt{3}A}{2}\sin\theta = -v_{Bo} \end{aligned}\right\} \tag{3.28}$$

Find Zero sequence signal voltage

$$v_{no} = \frac{A}{2}\cos\theta = \frac{1}{2}v_{An} \tag{3.29}$$

Sector 6

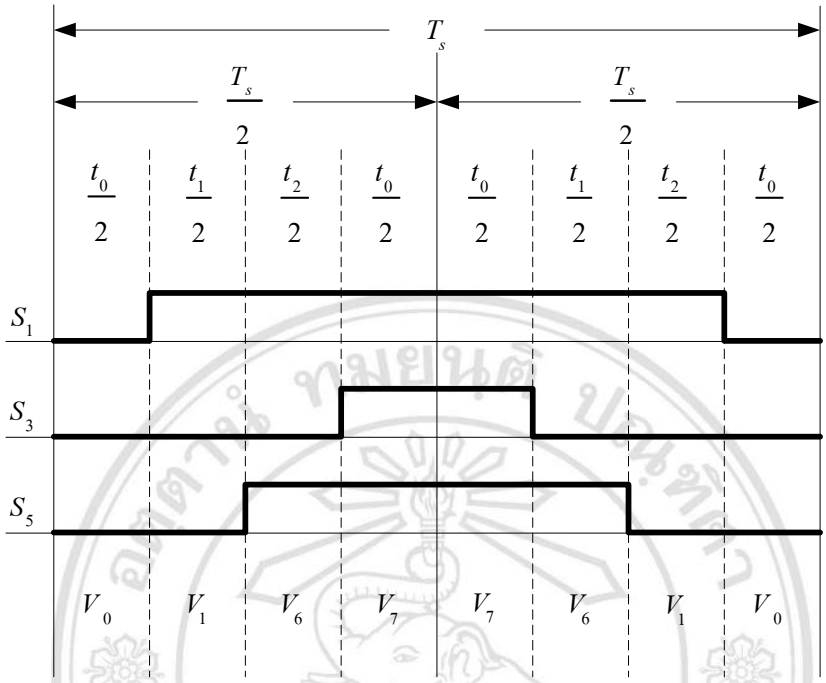


Figure 3.11 Switching pattern in sector 6

Calculate v_{Ao}, v_{Bo} and v_{Co} use same formula in sector 1

$$\left.\begin{aligned} v_{Ao} &= \frac{\sqrt{3}A}{2}\cos\left(\theta+\frac{\pi}{6}\right) \\ v_{Bo} &= -\frac{\sqrt{3}A}{2}\cos\left(\theta+\frac{\pi}{6}\right) = -v_{Ao} \\ v_{Co} &= \frac{3A}{2}\cos\left(\theta+\frac{2\pi}{3}\right) \end{aligned}\right\} \tag{3.30}$$

Find Zero sequence signal voltage

$$v_{no} = \frac{A}{2}\cos\left(\theta+\frac{2\pi}{3}\right) = \frac{1}{2}v_{Cn} \tag{3.31}$$

From finding a zero voltage the past six sector a summary given in

$$v_{no} = \frac{1}{2} median\left(v_{An}, v_{Bn}, v_{Cn}\right) \tag{3.32}$$

median is $max\left(v_{An}, v_{Bn}, v_{Cn}\right) + min\left(v_{An}, v_{Bn}, v_{Cn}\right)$

Voltage reference (v_{Ao}, v_{Bo} และ v_{Co}) has equal v_{no} added every voltage reference (v_{An}, v_{Bn} และ v_{Cn})

$$\left.\begin{aligned} v_{Ao} &= v_{An} + v_{no} \\ v_{Bo} &= v_{Bn} + v_{no} \\ v_{Co} &= v_{Cn} + v_{no} \end{aligned}\right\} \tag{3.33}$$

And then use v_{Ao}, v_{Bo} and v_{Co} to modulation with carrier-based pulse width modulation in Figure 3.12

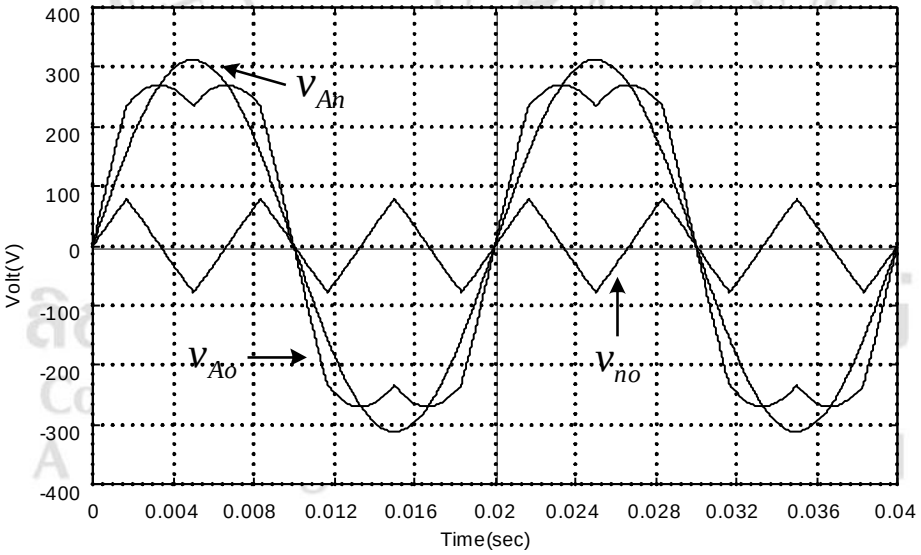


Figure 3.12 Voltage reference compare with v_{Ao}, v_{An} และ v_{no}

Improved carrier based PWM (CBPWM), detailed explanation of this algorithm is done in [25]. Basic voltage equations can be written as (3.34) from Figure 3.12:

$$\left.\begin{aligned} v_{af} &= v_{an} - v_{nf} \\ v_{bf} &= v_{bn} - v_{nf} \\ v_{cf} &= v_{cn} - v_{nf} \end{aligned}\right\} \tag{3.34}$$

where v_{af}, v_{bf} and v_{cf} are line to neutral voltages, $v_{an} - v_{cn}$ are pole voltages and v_{nf} is an offset of neutral leg, which can be controlled and modified similarly to the other legs. Equations (3.34) and (3.35) show maximum achievable output voltage and maximum offset voltage in the neutral leg in dependence on demanded phase voltages:

$$\left.\begin{aligned} \frac{-V_{dc}}{2} \le v_{af}, v_{bf}, v_{cf} \le \frac{-V_{dc}}{2} \\ \frac{-V_{dc}}{2} \le v_{nf} \le \frac{-V_{dc}}{2} \end{aligned}\right\} \tag{3.35}$$

$$\frac{-V_{dc}}{2} - V_{\min} \le v_{nf} \le \frac{-V_{dc}}{2} - V_{\max} \tag{3.36}$$

where $V_{\min} = \min(v_{af}, v_{af}, v_{af}), V_{\max} = \max(v_{af}, v_{af}, v_{af})$. And finally using $V_{\min}$ and $V_{\min}$ to create Zero sequence signal added to v_{af}, v_{bf}, v_{cf} (3.37) or $V_{f0} = -\frac{(V_{\min} + V_{\max})}{2}$ and wave form signal modulated shown in Figure 3.13

$$\left.\begin{aligned} &\frac{-V_{\max}}{2}, \textit{ when } V_{\min} > 0 \\ &\frac{-V_{\min}}{2}, \textit{ when } V_{\max} < 0 \\ &\frac{-(V_{\max} + V_{\min})}{2}, \textit{ otherwise} \end{aligned}\right\} \tag{3.37}$$

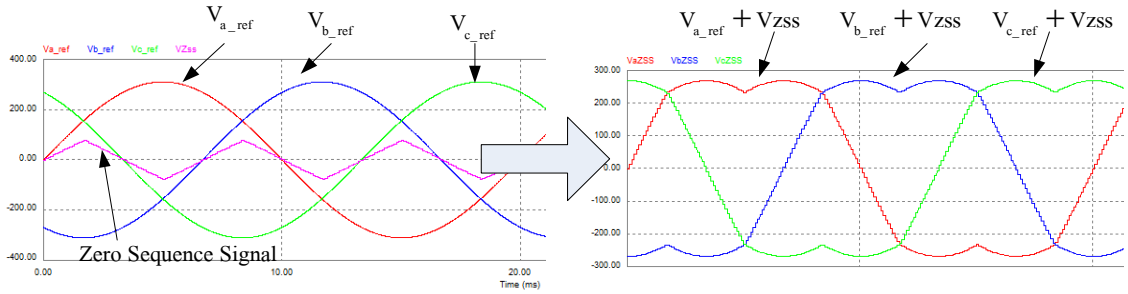


Figure 3.13 Wave form of Voltage for modulation to driving IGBT gate.

The switching times are determined by equations (3.37), which are common equations for carrier based PWM:

$$\left.\begin{aligned} T_a &= \frac{T_s}{2} + \frac{V_{an}}{V_{dc}}.T_s \\ T_b &= \frac{T_s}{2} + \frac{V_{bn}}{V_{dc}}.T_s \\ T_c &= \frac{T_s}{2} + \frac{V_{cn}}{V_{dc}}.T_s \\ T_d &= \frac{T_s}{2} + \frac{V_{dn}}{V_{dc}}.T_s \\ T_f &= \frac{T_s}{2} + \frac{V_{fn}}{V_{dc}}.T_s \end{aligned}\right\} \qquad (3.37)$$

In the 3-phase 4-leg system not only a neutral connection (Figure 3.14) but also the controllability of a zero sequence voltage. By using an offset voltage concept, a zero switching vector can be located at desired timing, so that the symmetrically aligned sequencing scheme can be achieved. Therefore, the PWM strategy using an offset voltage concept could be applied to the 3-phase 4-leg voltage source converter. In which 3D SVPWM can be implemented equally by a CBPWM by injecting a proper zero sequence function to its active modulating signals. Hence, the ON-time of the upper switch of respective legs can be simply implemented with a triangular carrier and the zero sequence signals as shown in Figure 3.13. And the result of simulation will show in next chapter.

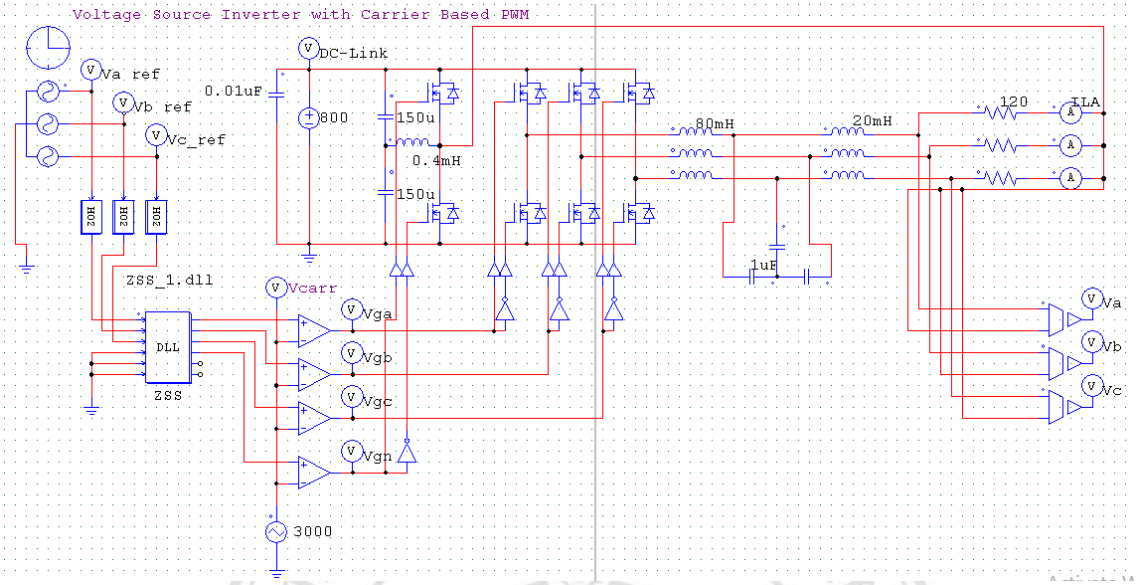


Figure 3.14 PSIM simulation circuit of A 3 Phase 4 Leg 4 Wire Voltage Source Inverter using carrier-based PWM technique

And this research added easy 7 sag signal algorithm (Figure 3.15) call ***Sag block***. with the algorithm, the signal can adjust magnitude percent sag depth (0-100%), number of phase to sag (1-3), point on wave of sags (0-360^{o}), phase shift and duration time of sag can be program via keypad or RS232 communication to microcontroller. In summary, the added algorithm it's easily to develop and implement to microcontroller.

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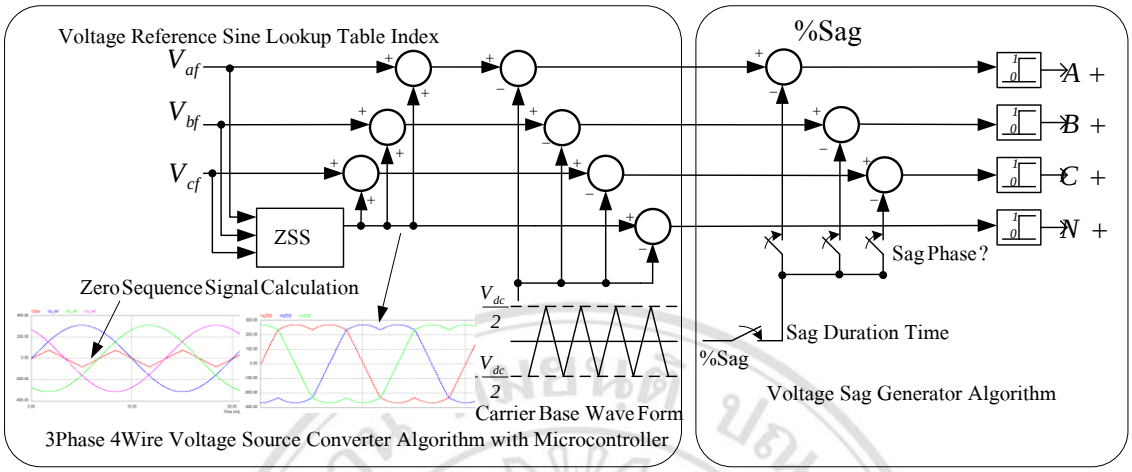


Figure 3.15 Zero sequence calculation, carrier base, %Sag and duration time modulation waveform.

In Equation 3.34 we can reduce or change modulation index m for make a % sags of normal voltage with 3.38 with multiply m in 0.1-0.9pu to v_{af}, v_{bf}, v_{cf} Voltage reference v_{af}, v_{bf}, v_{cf} are in sine lookup table 64 value in C programing language shown in Figure 3.16

$$\left.\begin{aligned} v_{af} &= m * v_{an} - v_{nf} \\ v_{bf} &= m * v_{bn} - v_{nf} \\ v_{cf} &= m * v_{cn} - v_{nf} \end{aligned}\right\} \qquad (3.38)$$

```
int sinetable[] = {0,3212,6393,9512,12539,15446,18204,20787,23170,25329,
27245,28898,30273,31356,32137,32609,32767,32609,32137,31356,30273,28898,
27245,25329,23170,20787,18204,15446,12539,9512,6393,3212,0,-3212,-6393,
-9512,-12539,-15446,-18204,-20787,-23170,-25329,-27245,-28898,-30273,
-31356,-32137,-32609,-32767,-32609,-32137,-31356,-30273,-28898,-27245,
-25329,-23170,-20787,-18204,-15446,-12539,-9512,-6393,-3212,0};
```

Figure 3.16 Sine lookup table 64 value.

The simulation of Voltage sags generator in this research using PSIM and show circuit diagram in Figure 3.17

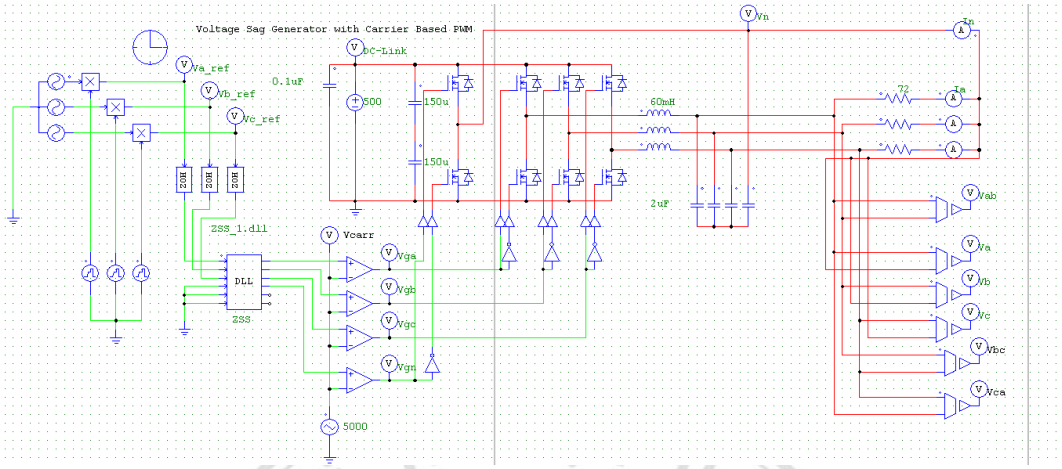


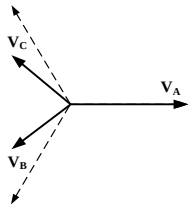
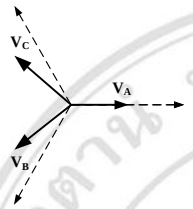
Figure 3.17. Circuit simulation of CBPWM voltage sag generator

The all of algorithm of voltage sag signal created by equation in [3.38]. For the example is shown in Figure 3.18 the phasor diagram of voltage sag type C or G [Table 3.1], the parameter of this type consist of phase angle-jump (ϕ,ϕ_b,ϕ_c), the magnitude drop in phase B and phase C duration time. This phasor is shown the magnitude and phase angle, the duration time can be input by user and this type is use almost variable are in control voltage sags generate signal.

The three phase voltage signal use shift register value in array of sine lookup table use C language technique. The dsPIC microcontroller has 16bit register value 0-65535 plus sign we can shift with array in heximal value is 0x0000 is 0 degree 0x5555 is 120 degree and 0xAAAA is 240 degree .

With this technique we can shift phase like and voltage sags type C or G with shift from normal value lookup table index. In this reseach we added 30 degree lag or lead phase shift angle with sine lookup table 0x1555

Table 3.1 Voltage Sags Type C and G

Type C Phase to Phase Faults		$V_A = 1$ $V_B = -\frac{1}{2} - \frac{1}{2} jV\sqrt{3}$ $V_C = -\frac{1}{2} + \frac{1}{2} jV\sqrt{3}$	Phase to phase fault Star-connected Load
Type G Two-phase-to-ground faults		$V_A = \frac{2}{3} + \frac{1}{3}V$ $V_B = -\frac{1}{3} - \frac{1}{6}V - \frac{1}{2} jV\sqrt{3}$ $V_C = -\frac{1}{3} - \frac{1}{6}V + \frac{1}{2} jV\sqrt{3}$	Two Phase to ground fault Delta-connected Load

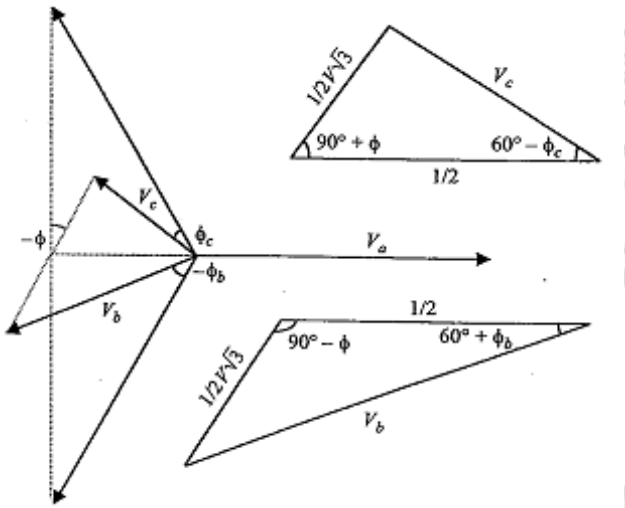


Figure 3.18 The phasor diagram for voltage sag type C.

3.5 Flowchart and Software Algorithm of Sag Type

In Figure 3.19 shown the flowchart of voltage sag algorithm based on IEC-61000-4-11 and SEMI F47. The algorithm program use 5 parameter to create the voltage sag as follow:

- **Phase** [1-3] number of phase of voltage sag or No. of m 0.1-0.9pu multiply

- **Sags** [0-100%] magnitude of voltage sag

- **Time** [0-9999ms] duration time of voltage sag from International standard test

- **Angle** [0-360 º] point on wave of voltage sag

- **Phase angle jump** [30º]

The duration time of voltage sag use dsPIC Timer1 16bit module interrupt every 1ms. Duration time is minimum 1mS and maximum 9999mS upon user configuration. And interrupt Timer1 write in C code :

```
void __attribute__((__interrupt__)) _T1Interrupt( void )
{
    IFS0bits.T1IF = 0;          // reset Timer 1 interrupt flag
        if(delaySag<=0){
            Flags.Sag = 0;
            Flags.Reduce = 0;
            SagSignal = 0;
            T1CONbits.TON = 0;
            delaySag=sagTemp;
        }else delaySag--;
}
```

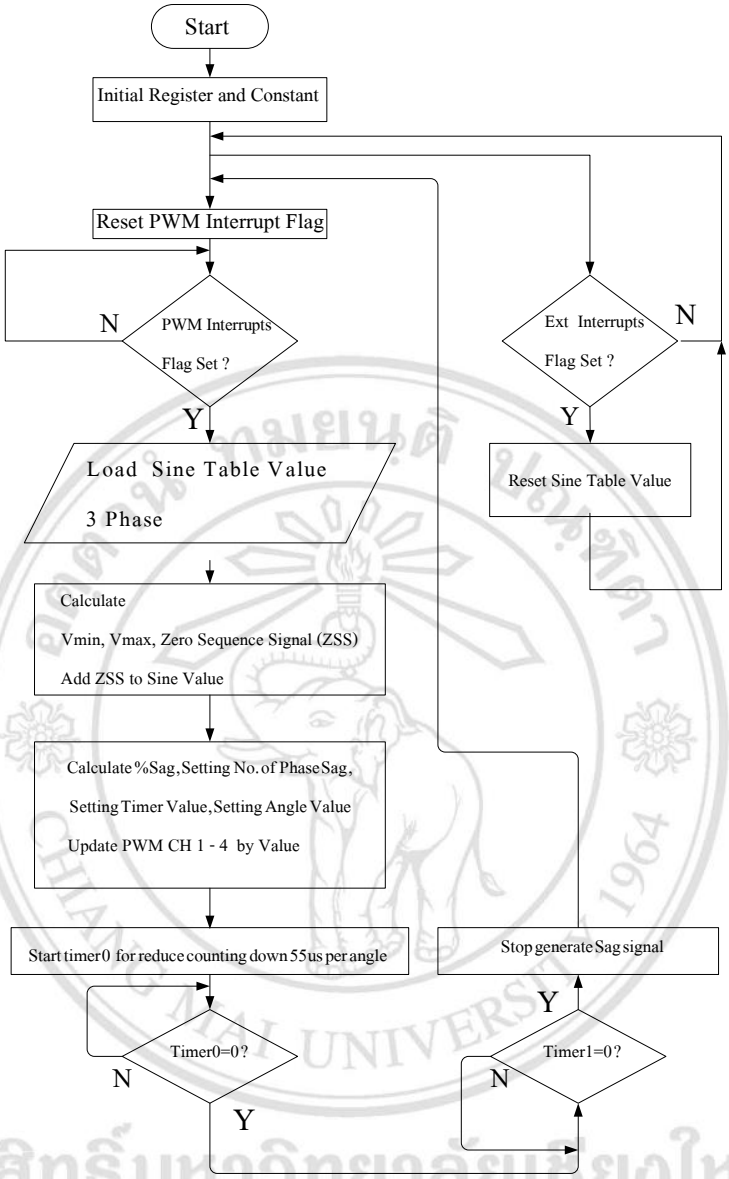


Figure 3.19 Flowchart of generate voltage sag signal.

3.6 The MATLAB m-file and GUI plot simulation.

The SagWave based on MATLAB graphic user interface (GUI) (Figure 3.20) the SagWage GUI had designed consist of:

- The axis-1 for show the 3-phase voltage
- Sag type for selected the voltage sag type (single-phase, two-phase and three-phase)

- Point on wave in degree.
- Sag duration time for period time of voltage sag.
- Magnitude of voltage (A, B and C phase), user had used value box or slider bar.
- Phase angle jump of voltage sag on A, B or C phase.
- The axis-2 for show the vector of A, B and C phase.
- The button “Plot” for generated the voltage sag waveform or command line.

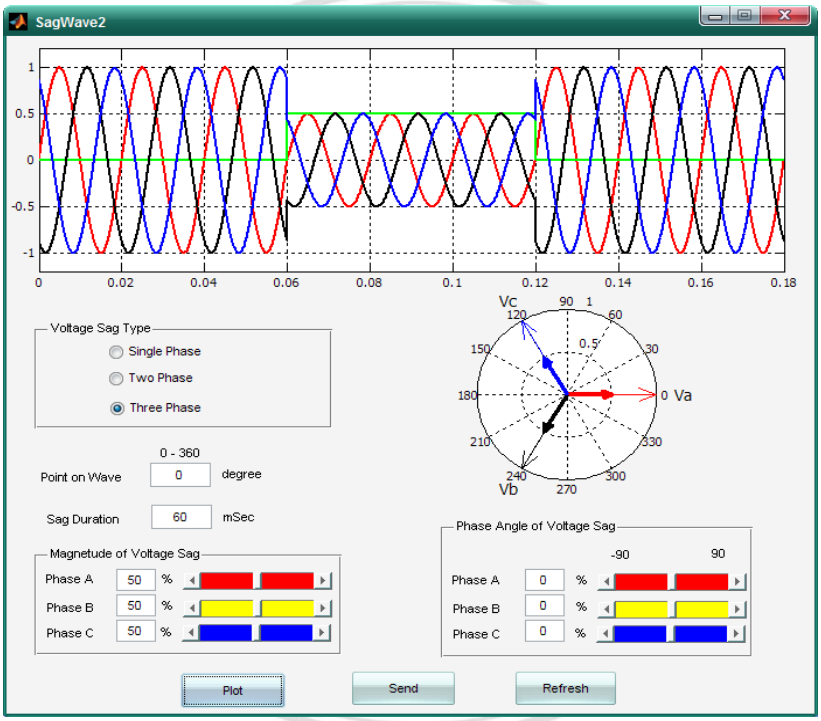


Figure 3.20 SagWave software create from MATLAB GUI [26]

3.7 Implementation with microcontroller

The operation of voltage sags generator is controlled by dsPIC30F6010a (dsPIC30F) made by Microchip. The dsPIC30F devices contain extensive digital signal processor (DSP) functionality within a high-performance 16-bit microcontroller (MCU) architecture. The dsPIC30F core is a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including support for DSP. The dsPIC30F has 16-bit compare/PWM output functions. It has 8 PWM output channels which can be selected output mode as complementary or independent. The PWM output signal in dsPIC30F can be generated by using center aligned modes as shown in figure 3.21

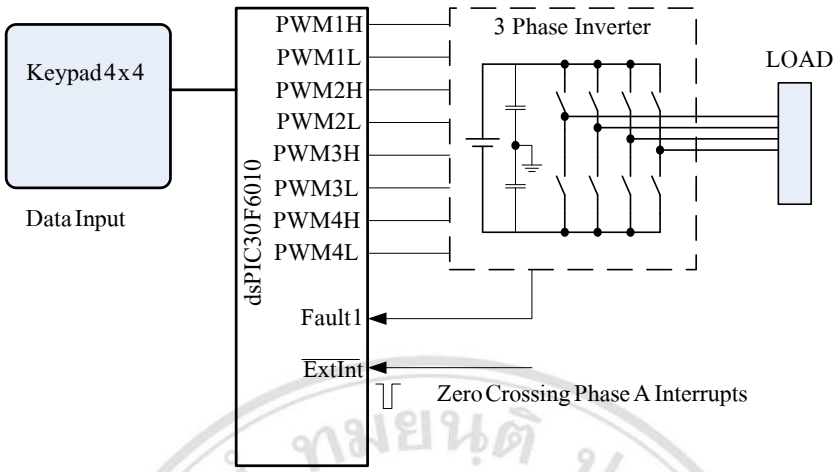


Figure 3.21 dsPIC30F6010a Microcontroller block diagram.

The practical implementation method of the space vector PWM (SVPWM) with a triangular carrier wave (CBPWM) was proposed using the offset voltage concept in [24] and diagram in Figure 3.3 The switch states of each leg are determined by comparison between the determined pole voltages in (3.1) and a triangular carrier wave, and then naturally the optimum switching sequence is obtained as shown in Figure 3.22

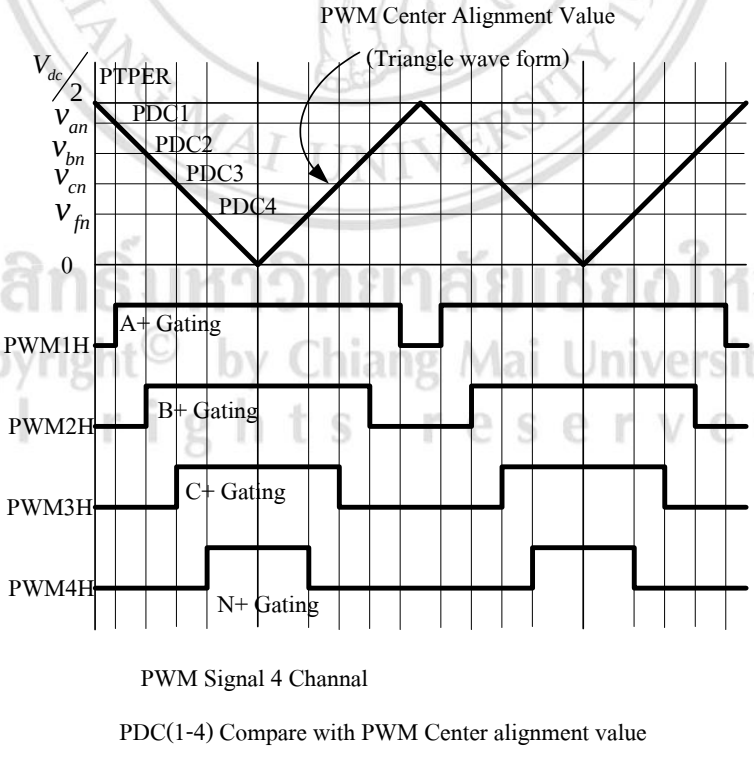


Figure 3.22 Carrier-Based PWM technique from dsPIC microcontroller.

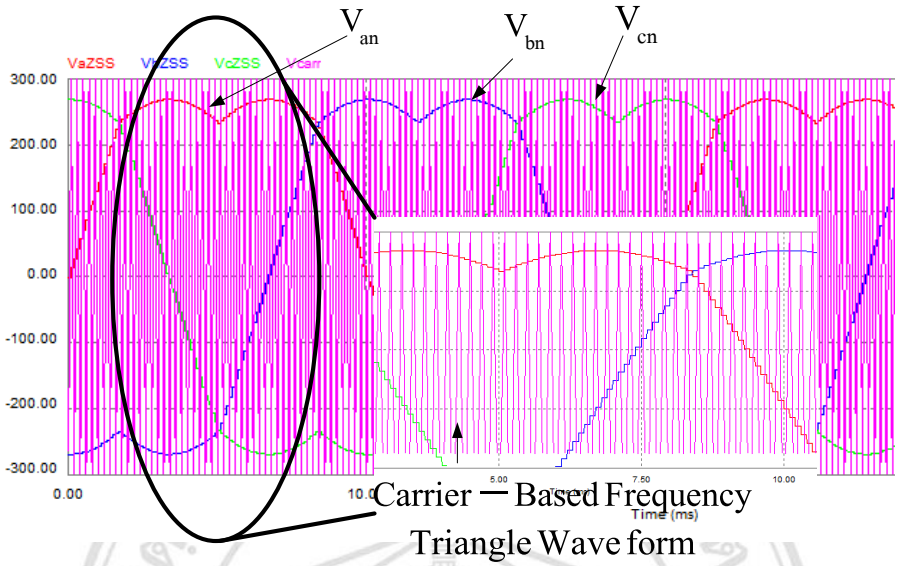


Figure 3.23 PSIM simulation signal added $V_{a\_ref} + Vzss$ Modulation with Triangle wave form.

3.8 Microcontroller dsPIC C30 software code

Normal AC voltage output with modulation index from C code microcontroller running program and get sine value from sine lookup table and compare triangle carrier-based with PWM module center alignment function every PWM register count up-down finish PWMInterrupt will happen. The interrupt has every $1/F_{SW} = 1/5kHz = 0.0002\,Sec.$ or 200uS. In PWMInterrupt has a program sag algorithm for calculate AC voltage output, duration time, number of phase sag happen, point on wave and phase angle jump.

```
void __attribute__((__interrupt__)) _PWMInterrupt(void)
{
        Phase += Delta_Phase;
        Phase_Offset = _0_DEGREES;
        Multiplier = sinetable[(Phase + Phase_Offset) >> 10];
  if((!Flags.Reduce)&&(Flags.Sag)&&(Multiplier==0)&&(Multiplier1>=0)){
    T2CONbits.TON = 1;
  }
        asm("MOV _Multiplier, W4");
        asm("MOV _PTPER, W5");
        asm("MOV _Amplitude, W6");
        asm("MOV #_ResultA, W0");
        asm("MPY W4*W5, A");
        asm("SAC A, W7");
        asm("MPY W6*W7, A");
        asm("SAC A, [W0]");
  Multiplier1 = Multiplier;
```

C30 code for reduce AC output voltage when voltage sags happen with SagDrop register.

```
    if(Flags.Reduce){
                                        switch(PhaseSag){
                                        case 1: {
                                                        ResultA = (int)ResultA*SagDrop;
                                                       }break;
                                        case 2: {
                                                        ResultB = (int)ResultB*SagDrop;
                                                        ResultC = (int)ResultC*SagDrop;
                                                       }break;
                                        case 3: {
                                                        ResultA = (int)ResultA*SagDrop;
                                                        ResultB = (int)ResultB*SagDrop;
                                                ResultC = (int)ResultC*SagDrop;
                                                       }break;
                                        }
            }
```

C30 code for delay duration time of voltage sags happen. The time1 set interrupt every 1ms.

```
void __attribute__((__interrupt__)) _T1Interrupt( void )
{
    IFS0bits.T1IF = 0;                  // reset Timer 1 interrupt flag
            if(delaySag<=0){
          Flags.Sag = 0;
                    Flags.Reduce = 0;
          SagSignal = 0;
                    T1CONbits.TON = 0;
          delaySag=sagTemp;
            }else delaySag--;
}

//-------- Timer 1 Initial ----------------------------------------------
   T1CON = 0;                 // ensure Timer 1 is in reset state
   IFS0bits.T1IF = 0;         // reset Timer 1 interrupt flag
   IPC0bits.T1IP = 1;         // set Timer1 interrupt priority level to 1
   IEC0bits.T1IE = 1;         // enable Timer 1 interrupt
   PR1 = 7372;                // set Timer 1 period register
   T1CON = 0x0000;
```

C30 code for delay time of point on wave voltage sags happen. The time2 set interrupt every 55us (1 degree of 360degree/20ms 50Hz).

```
void __attribute__((__interrupt__)) _T2Interrupt( void )
{
    IFS0bits.T2IF = 0;
            if(delayAngleSag<=0){
          Flags.Reduce = 1;
          SagSignal = 1;
                    T1CONbits.TON = 1;
```

```
                    T2CONbits.TON = 0;
          delayAngleSag=sagAngleTemp;
            }else   delayAngleSag--;
}

//-------- Timer 2 Initial ------------------------------------------------
   T2CON = 0;                  // ensure Timer 2 is in reset state
   IFS0bits.T2IF = 0;          // reset Timer 2 interrupt flag
   IPC1bits.T2IP = 2;          // set Timer2 interrupt priority level to 2
   IEC0bits.T2IE = 1;          // enable Timer 2 interrupt
   PR2 = 409;                  // set Timer 2 period register Timing/Degree
   T2CON = 0x0000;
```

And zero Sequence Signal Calculation from sine lookup table v_{af}, v_{bf}, v_{cf} reference.

```
min_value(int x1, int x2, int x3){
int min;
   min = x1;
   if ( x2 < min ) min = x2;
   if ( x3 < min ) min = x3;
return min;
}

max_value(int x1, int x2, int x3){
int max;
   max = x1;
   if ( x2 > max ) max = x2;
   if ( x3 > max ) max = x3;
return max;
}

ZSS(int min,int max){
int ZSS;
            ZSS=-(max+min)/2;                    // ZSS=((1-max)/2)+((-1-min)/2);
return ZSS;
}
```

3.9 Power electronics part of inverter design

In this research use power electronics and switching PWM frequency shown in Table 3.2 using for test electrical equipment with load about 1KVA three phase balance/unbalance or International standard IEC61000-4-11 limitation of current less than 16A. and test with international standard SEMI F47

Table 3.2 Parameter power part used in experiment hardware setup for voltage sag generator.

Controllable switches	DC bus voltage	Carrier frequency	R*	C Filter	L Filter
IRG4PH40UD (1200V 21A)	500 V	5 kHz	72Ω	2μF	40mH

* Used $R_{a\text{-}c}$ 72Ω for balance load, used $R_{b\text{-}c}$ 38Ω for unbalance load

3.10 Design AC output LC low pass filter

The purpose of adding a filter to the output of the DC/AC inverter is to improve its voltage output. This output is influenced by PWM switching technique and that is why it needs additional filtering. For each filter configuration and each filter order, two different topologies are considered: even (with inductance at input side of the filter) and odd (with capacitance at input side of the filter).

Some filter topologies (which end with capacitance: second order even, third order odd and fourth order even) produce smaller THD of load current than other filter topologies (which end with inductance: second order odd, third order even and fourth order odd). The cut-off frequency of all simulated low-pass filter configurations was 50Hz. However, it is found that fourth order even filter introduces instability in output voltage of the Voltage Sags Generator. Therefore, second order filter is chosen as optimal filter configuration.

The influence of output filter on the voltage sags generator performances is found to be significant. Generally, with increasing the filter order output voltage waveform is less distorted. However, higher order filters are more “load dependant”, more expensive and more difficult to construct, and they introduce larger phase shift and delay in filtered output signal. L and C from a 2nd order filter with -40dB/dec attenuation to switching ripples with the 5kHz switching frequency f_{res} is selected as 750Hz for less than 15% of voltage ripple

at switching frequency. In this research was selected L_f = $40mH$ and C_f = $2uF$. The resonance frequency f_{res} is

$$f_{res} = \frac{1}{2\pi\sqrt{L_f C_f}}$$

$$f_{res} = \frac{1}{2\pi\sqrt{40mH \times 2\mu F}} = 562.698 \text{ Hz}$$

The resonance frequency is less than 12% of switching frequency.

In order to test the sensitivity of electrical equipment to such momentary voltage disturbance or voltage sag, a particular device is needed. To this goal, it is necessary to have a voltage sag generator, that is, a device or equipment capable of generating the suitable voltage-time profiles. Voltage sag generator (VSG) is a signal generator that can produce voltage sags of desired characteristics in order to test and identify equipment responses to such voltage disturbances.

Generally, current power quality standards define and describe voltage sags by only two parameters which are magnitude and duration. All these voltage sag characteristics introduced by the VSG should be fully controlled and easily repeated in systematic experiments. The influence of these voltage sag parameters on certain equipment can be significant.

Summary

In this chapter, the method of design, simulation, implementing and experiment the Voltage Sags Generator and result and experiment will discuss in next chapter.