

บรรณานุกรม

- [1] ชานินทร์ สุเชียง, “การพัฒนาโปรแกรมເອົ້າສໍາຮັບວົງຈະດິຈິຕອລໂດຍໃຊ້ວິທີຮາຍການລດທອນ”, ວິທະຍານິພັນຮົວສົກຮຽມຄາສຕຣມຫາບັນທຶກ ມາວິທາລັຍເຊີ່ງໃໝ່, 2543.
- [2] ເອກະພແສງອິນທີ່, “ການທົດສອບວົງຈະຮ່ວມໝາດໃໝ່ນາກ”, (An Overview of Testing VLSI Chip), ວາງສາວວິສົກຮຽມຄາສຕຣ໌ ມາວິທາລັຍເຊີ່ງໃໝ່, Vol. 5, No. 2, Nov 1995, pp 95-104
- [3] Aspvall, B., Plass, M., and Tarjan, R., “A Linear-Time Algorithm for Testing the Truth of Certain quantified Boolean Formulas”, Information Processing Letter, 8,1979, pp 121-123.
- [4] Auth, E. and Schulz, M. H., “A Test-Pattern-Generation Algorithm for Sequential Circuits”, IEEE Design & Test of Computers, Vol 8, Iss. 2, 1991, pp72-85
- [5] Brglez, F.,Bryan, D. and Kozmin’ski, K., “Combinational Profiles of Sequential Benchmark Circuits ”, IEEE Proc. Int. Symp. On Circuits and Systems, Portland OR, USA,1989, pp 1929-1934
- [6] Brglez, F. and Fujiwara, H., “A Neutral Netlist of 10 Combinational Benchmark Circuits and a Target Translator in Fortan”, IEEE Proc. Int. Symp. Circuits and Systems, Special Session on ATPG and Fault Simulation, Kyoto, Japan, June 1985
- [7] Cook, S. A., “The Complexity of Theorem Proving Procedures”, In Proceedings of the Third Annual ACM Symposium of Theory of Computing. ACM, 1971
- [8] Friedman, D., Menon, P. R., “Fault Detection in Digital Circuit”, Bell Telephone Laboratory Inc., Prentice-Hall Inc., New Jersy, USA, 1971
- [9] Hamzaoglu, I., and Patel, J. H.,”New Technique for Deterministic Test Pattern Generation”, VLSI Test Symposium, 1998. Proceedings, 16th IEEE, 1998, pp 446-452
- [10] Joseph, M., et al., “An Analysis of Fault Partitioned Parallel Test Generation”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol 15, No.5, May, 1996, pp 517-534
- [11] Konuk, H and Larrabee, T., “Exploration of Sequential ATPG Using Boolean Satisfiability”, in Proceedings of Design Automation Conference, 1993,pp 458-462

- [12] Larrabee, T., "Test Pattern Generation Using Boolean Satisfiability ", Transactions on Computer-Aide Design, IEEE, Vol. 11, No 6, Jan. 1992, pp 6-22
- [13] McCluskey, E. J., and Clegg, F.W., "Fault Equivalence in Combinational Logic Networks", IEEE Trans. on Computers, Vol. C-20, NO. 12, Dec 1971, pp. 1286-1293
- [14] Muehldorf, E. I., and Savker, A. D., "LSI Logic Testing – An Overview", IEEE Trans. on Computers Vol 30., No. 1, Jan 1981, pp. 1- 17.
- [15] Niermann, T., and Patel, J. H., "HITEC: a test generation package for sequential circuits", Design Automation EDAC., Proceeding of the European Conference on, 1991, pp. 214-218
- [16] Niermann, T., et al., "Test Compaction for Sequential Circuits", Transactions on Computer-Aide Design, IEEE, Vol. 11, No. 2, Feb. 1992, pp 260-270
- [17] Rogel-Favila, B., "Model-Based Fault Diagnosis of Digitals", Ph. D., Thesis, Dept. of Electrical Engineering, Imperial Colledge of Science, Technology and Medicine, University of London, May 1991.
- [18] Roth, J. P., Bouricius, W. G. and Schneider, P. R. , "Programmed Algorithm to Compute Tests to Detect and Distinguish between Failures in Logic Circuits", IEEE Transactions on Electronic Computers, Vol EC-16, No. 5, Oct 1967, pp 567-580.
- [19] Sang-In, A., "Novel Algorithm for Automatic Test Pattern Generation in Digital Circuits", Ph. D. Thesis, Dept. of Electrical Engineering, Imperial Colledge of Science, Technology and Medicine, University of London, UK., May 1994.
- [20] Schulz, M. H., Trischler, E. and Sarfert, T. M., "SOCRATES: A Highly Efficient Automatic Test Pattern Test Pattern Generation System", IEEE Transactions on Computers, Vol. C-22, No. 11, Nov. 1973, pp 1008-1015
- [21] Thomas, A., S., "Data Structures, Algorithms & Software Principles in C", Addison-Wesley Co., 1995
- [22] To, K., "Fault Folding for Irredundant and Redundant Combinational Circuits", IEEE Transactions on Computers, Vol. C-22, No. 11, Nov. 1973, pp1008-1015
- [23] Waicukauski, J. A., et al., "Fault Simulation for Structured VLSI", VLSI Design, 1985, VI, pp. 20-32.